MB Booting and ASUS ASIC

Dec. 20, 2002

CSC / ASUS

AGENDA

1. ACPI states and MB Bootup.

2. Determination of
   CPU Vcore,
   CPU Core Frequency,
   CPU Frequency Multiplier.

3. Wake on LAN,
   Wake by KB,
   Wake On Ring,
   Wake On USB,
   AC Power Loss Restart.

4. POST

1. ACPI states and MB Bootup.

ACPI States

What is ACPI ?

- Advanced Configuration and Power Interface

ACPI

- ACPI evolves the existing collection of power management BIOS code, APM APIs, PNPBIOS APIs, and so on into a well-specified power management and configuration mechanism. It provides support for an orderly transition from existing (legacy) hardware to ACPI hardware, and it allows for both mechanisms to exist in a single machine and be used as needed.
- Further, new system architectures are being built that stretch the limits of current Plug and Play interfaces.
- ACPI evolves the existing motherboard configuration interfaces to support these advanced architectures in a more robust, and potentially more efficient manner.

ACPI States

Global System States

1. G3 - Mechanical Off State

ATX Unpluged

Battery Power Only

2. G2 / S5 - Soft Off

ATX pluged

+5V Standby and Battery

3. G1 - Global Sleeping State

S1 : No system context is lost

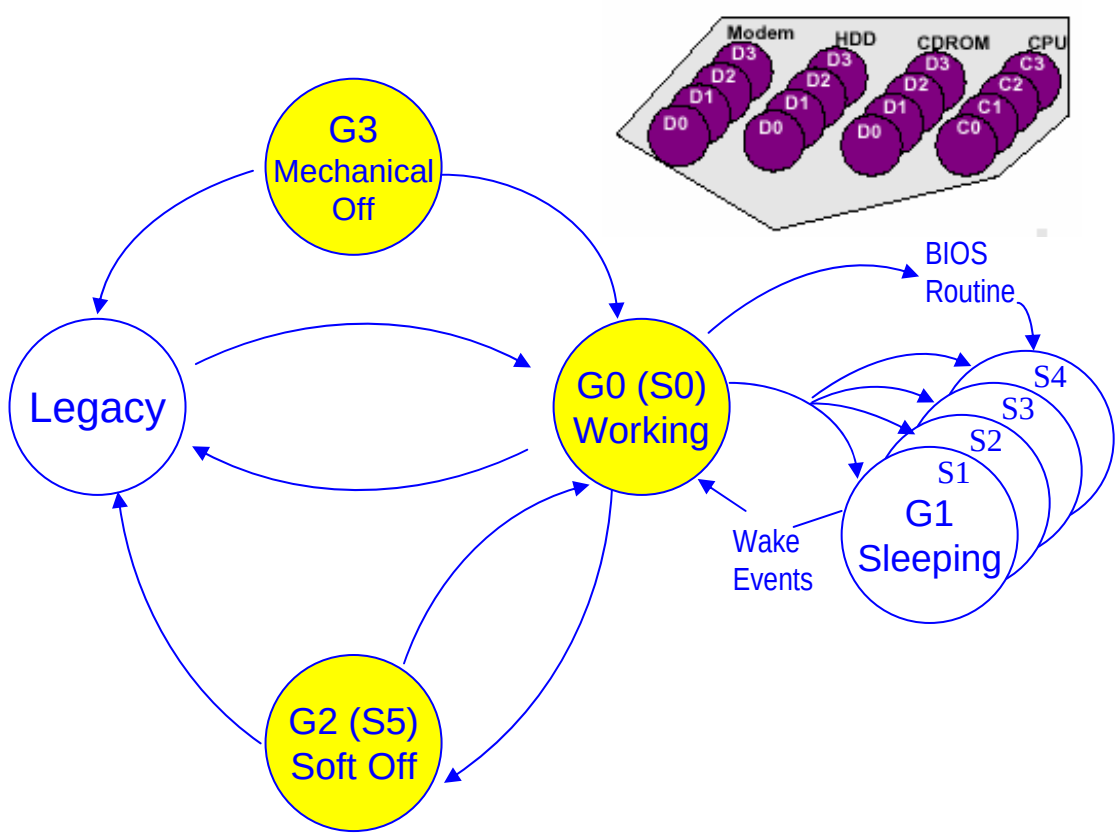
S2 : Cache context is lost

S3 : CPU, cache, and chipset context is lost. Memory is maintained.

Suspend To RAM (STR)

S4 : system context is maintained in Non-volatile storage.

Suspend To Disk (STD)



4. G0 - Global Working State

Full running

CPU States

C0 , C1 , C2 , C3

Global System States

1. G3 - Mechanical Off State

ATX Unpluged , Battery Power Only

2. G2 / S5 - Soft Off

ATX pluged , +5V Standby and Battery

3. G1 - Global Sleeping State

S1 : No system context is lost ,

S2 : Cache context is lost

S3 : Suspend To RAM (STR) ,

S4 : Suspend To Disk (STD)

4. G0 - Global Working State

Summary of Global Power States

Global System State	Software Runs	Latency	Power Consumption	OS restart required	Safe to disassemble computer	Exit state electronically
G0 – Working	Yes	0	Large	No	No	Yes
G1 – Sleeping	No	>0, varies with sleep state.	Smaller	No	No	Yes
G2/S5 - Soft Off	No	Long	Very near 0	Yes	No	Yes
G3 – Mechanical Off	No	Long	RTC battery	Yes	Yes	No

Note that the entries for G2/S5 and G3 in the Latency column of the above table are "Long." This implies that a platform designed to give the user the appearance of "instant-on," similar to a home appliance device, will use the G0 and G1 states almost exclusively (the G3 state may be used for moving the machine or repairing it).

Global System States

G0 - Global Working State

G1 - Global Sleeping State

S1 : No system context is lost

- ➔ the STPCLK# signal goes active to the processor.
- ➔ CPU performs a Stop-Grant cycle.
- ➔ Cache coherency is maintained.

S2 : Cache context is lost

- ➔ Not supported by ICH

S3 : Suspend To RAM (STR)

- ➔ System context is maintained in system memory.
- ➔ All clocks stop except RTC clock.
- ➔ Power is shut off to non-critical circuits. Memory is retained, and refreshes of DRAM continues.

S4 : Suspend To Disk (STD)

- ➔ System context is maintained on the disk.
- ➔ All power is shut off, except for the circuits to restart
- ➔ Externally appears same as S5, but may have different wake events.

G2/S5 - Soft Off

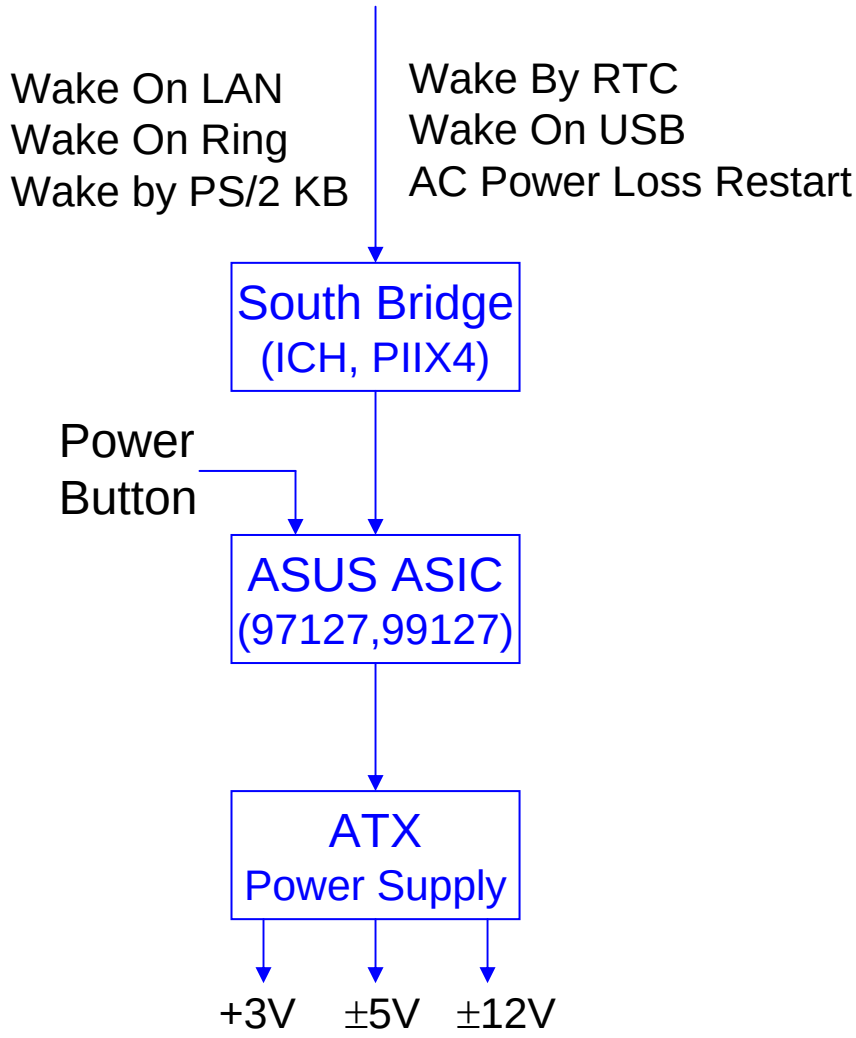
S5 : Soft Off

- ➔ System context is not maintained.
- ➔ All power is shut off except for the circuits to restart.
- ➔ A full boot is required when waking.

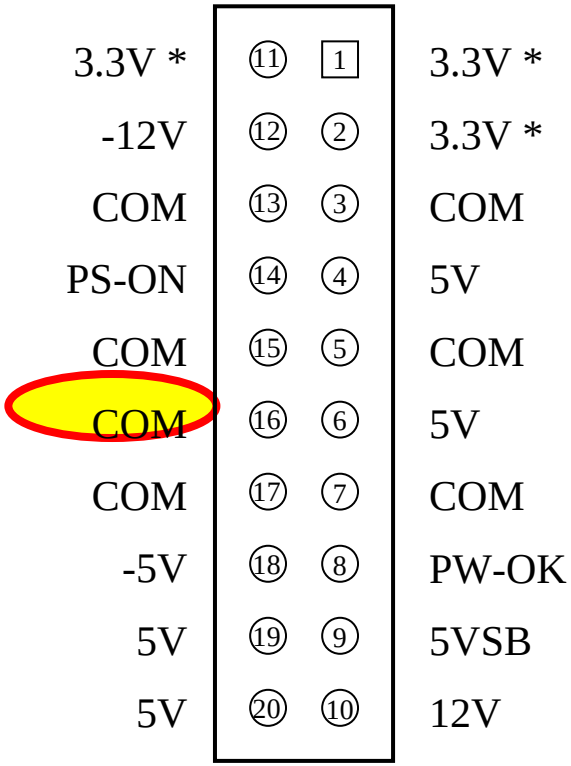
G3 - Mechanical Off

- ➔ All power is shut off except for RTC.
- ➔ No wake events are possible.

MB Bootup


Wake On LAN
Wake On Ring
Wake by PS/2 KB
Wake By RTC
Wake On USB
AC Power Loss Restart
South Bridge
(ICH, PIIX4)
Power
Button
ASUS ASIC
(97127,99127)
ATX
Power Supply
+3V
±5V
±12V

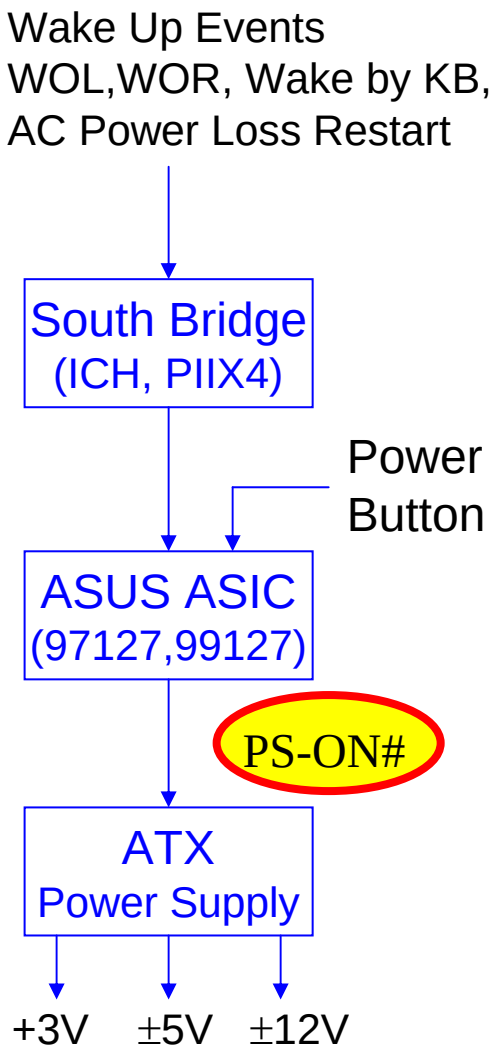
ATX Power Supply



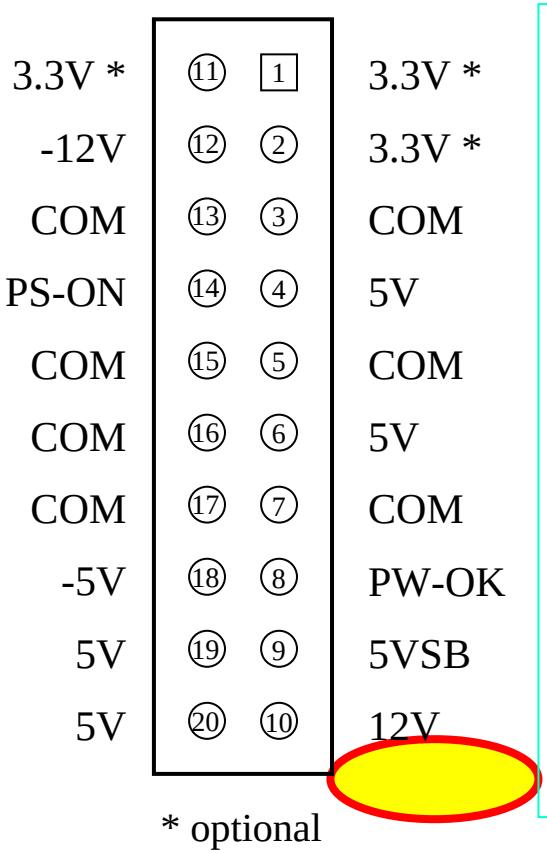
* optional

PS-ON is an active low signal that turns on all of the main power rails including 3.3V, 5V, -5V, 12V, and -12V power rails.

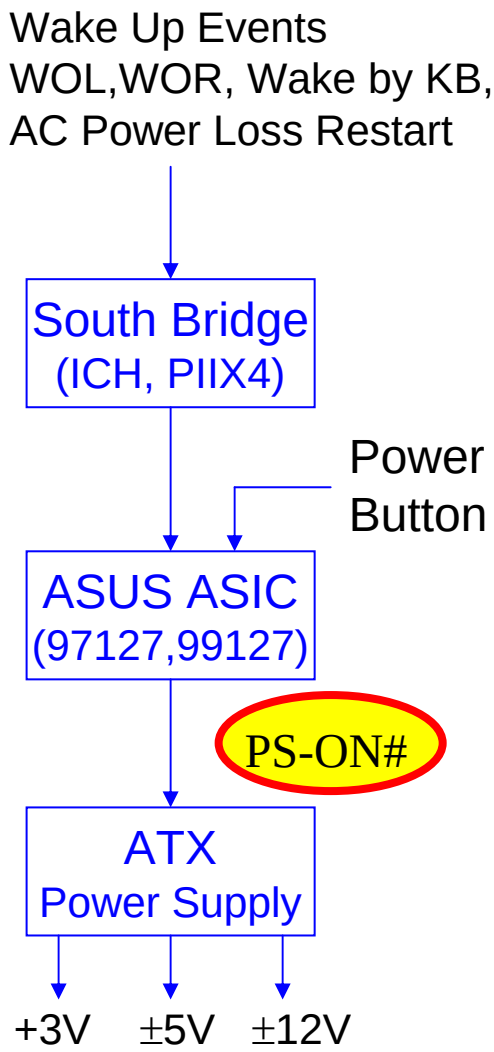
When this signal is held high by the PC board or left open circuited, outputs of the power rails should not deliver current and should be held at a zero potential with respect to ground. Power should only be delivered to the rails if the PS-ON signal is held at ground potential. This signal should be held at +5VDC by a pull-up resistor internal to the power supply.



ATX Power Supply

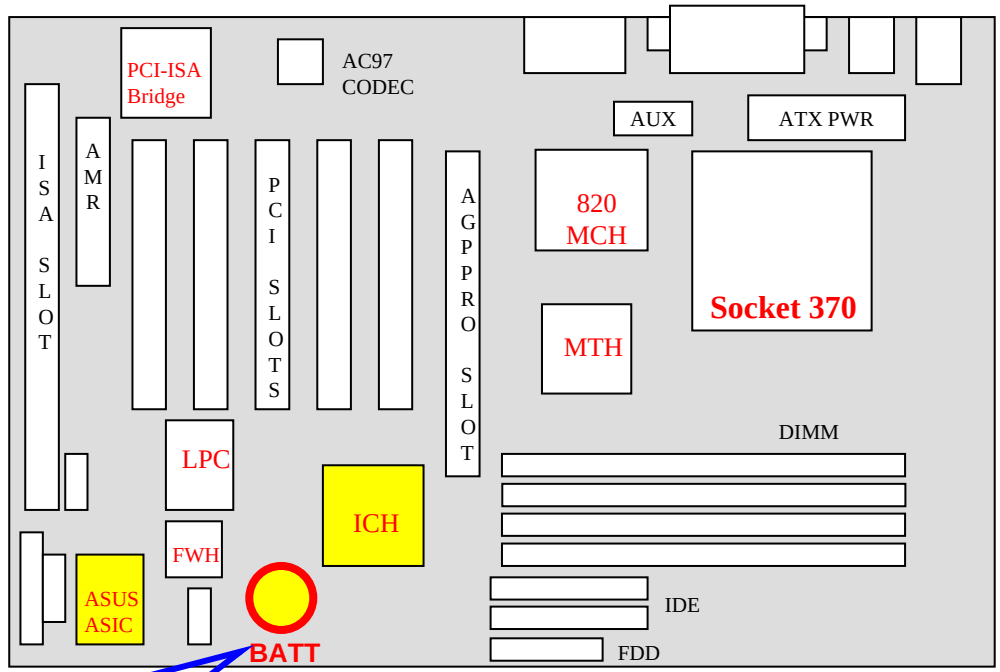


5VSB is a **standby** voltage that may be used to power circuits that require power input during the powered down state of the power rails. The 5Vsb pin should deliver 5V at a minimum of 10mA for PC board circuits to operate. Conversely, PC boards should draw no more than 10mA maximum from this pin unless a power supply with higher current capabilities is clearly specified. This power may be used to operate circuits such as soft power control. For future implementation it is recommended that the 5Vsb line be capable of delivering 720mA. This increased current will be needed for future implementations with features such as <Wake on LAN>.

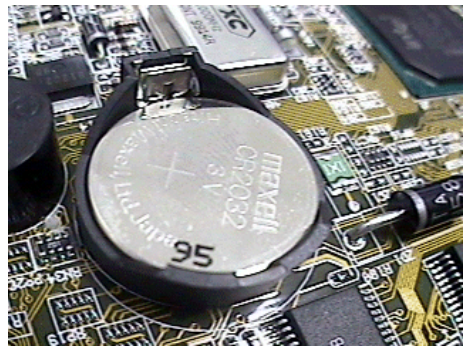


Motherboard in G3 Mechanical Off State

- When the motherboard is not connected to ATX power, there is only BATT(battery) power on board.
  - ACPI G3 mechanical state.
- There are still certain circuits on the board consuming the BATT power.
  - ICH
  - ASIC
  - other small discrete components.



Output : +3V

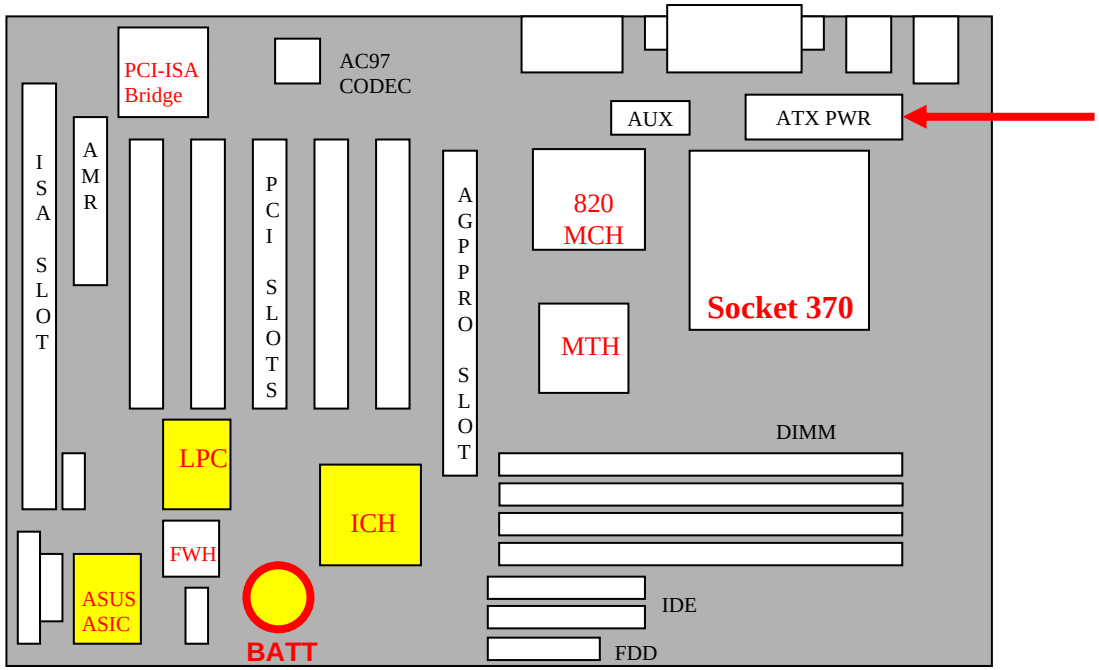


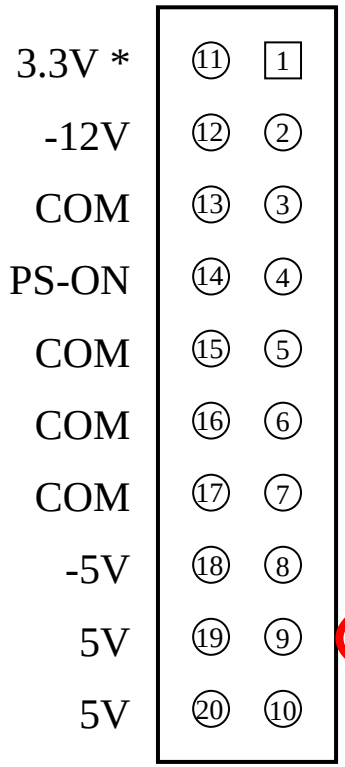
Functions in G3 state being maintained on board by the BATT power are :

- CMOS SRAM (in ICH)
- RTC (Real Time Clock) (in ICH)
- AC Power Loss Restart (in ICH)
- New CPU Detection (On board)
- Chassis Intrusion (On board)

Motherboard in G2 / S5 Soft Off State

Two Power planes :
1. BATT
2. Standby Power





* optional

COM
5V
COM
PW-OK
5VSB
12V

Voltage Regulator → +3VSB

Voltage Regulator → +1.8VSB

Voltage Regulator → +3VAux

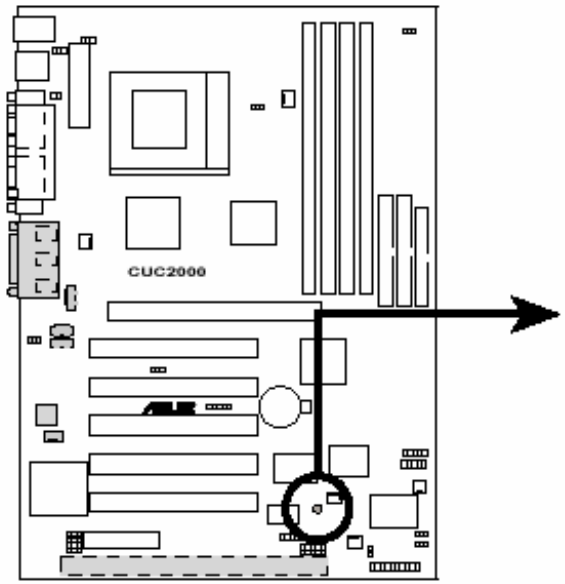
Supply to circuits for Wake Up Event :
WOR, WOL,
Wake Up by KB, USB

Motherboard in G2 / S5 Soft Off State

WARNING! Computer motherboards and expansion cards contain very delicate Integrated Circuit (IC) chips. To protect them against damage from static electricity, you should follow some precautions whenever you work on your computer.

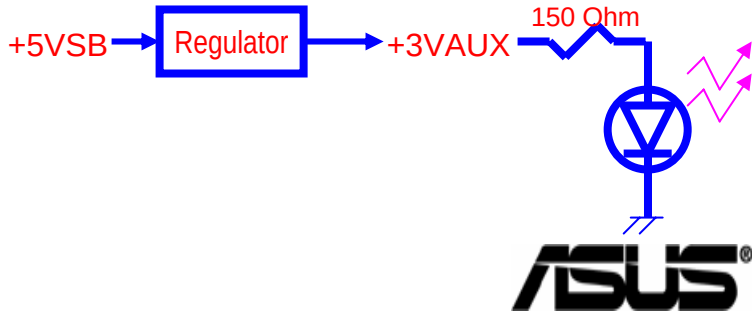
1. Unplug your computer when working on the inside.
2. Use a grounded wrist strap before handling computer components. If you do not have one, touch both of your hands to a safely grounded object or to a metal object, such as the power supply case.
3. Hold components by the edges and try not to touch the IC chips, leads or connectors, or other components.
4. Place components on a grounded antistatic pad or on the bag that came with the component whenever the components are separated from the system.
5. Ensure that the ATX power supply is switched off before you plug in or remove the ATX power connector on the motherboard.

WARNING! Make sure that you unplug your power supply when adding or removing system components. Failure to do so may cause severe damage to your motherboard, peripherals, and/or components. The onboard LED when lit acts as a reminder that the system is in suspend or soft-off mode and not powered OFF.



ON
Standby Power

OFF
Powered Off

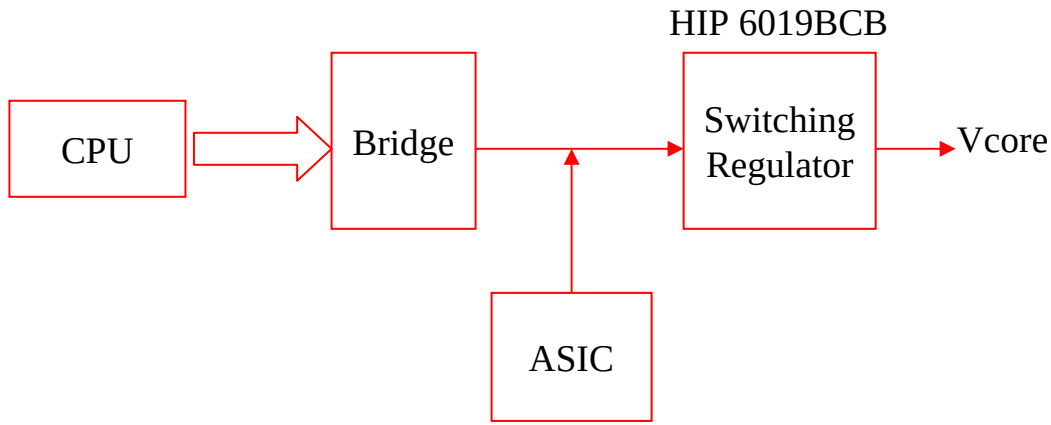


CUC2000 Onboard LED

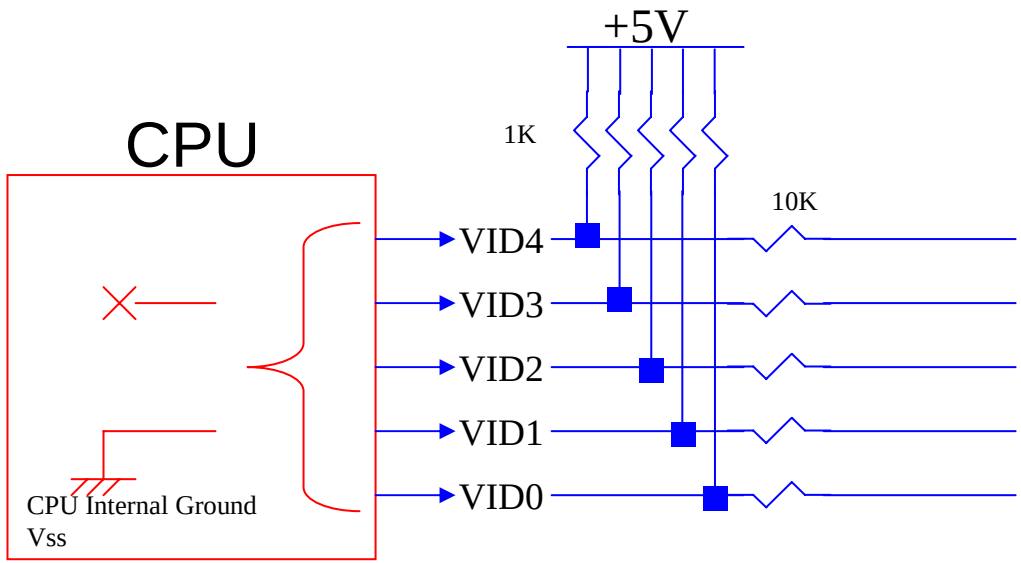
2. Determination of
CPU Vcore,
CPU Core Frequency,
CPU Frequency Multiplier.

CPU Vcore

- Klamath PII Later
  - 5 pins on the CPU to inform the motherboard what sort of core voltage it needs.
  - VID0
  - VID1
  - VID2
  - VID3
  - VID4



- The VID pins on the CPU are not output signals :
  - Internally connected to GND -- Low
  - Open circuit -- High



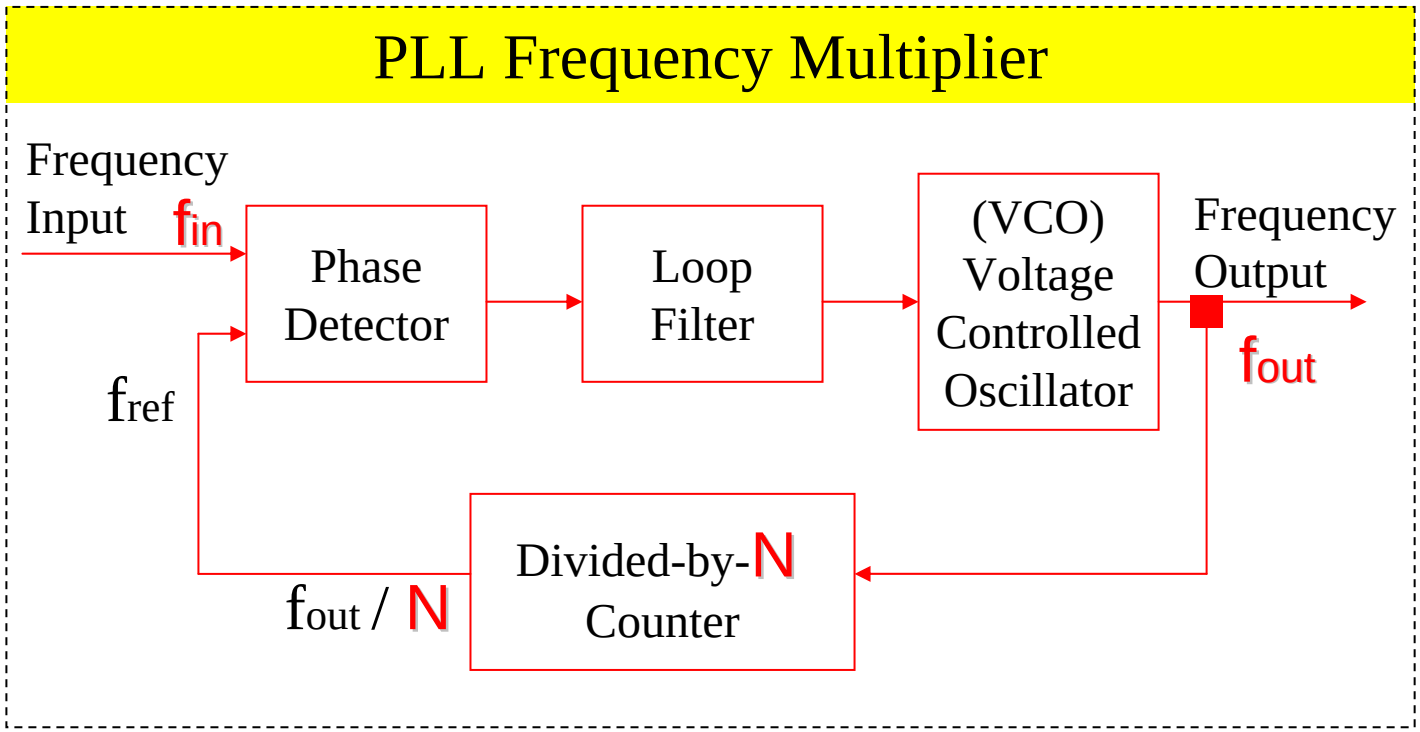
CPU Core Frequency

- PLL
  - Phase Lock Loop
- $f_{out} = N * f_{in}$

- f_{in} = FSB frequency

  N = Frequency multiplier setting
- f_{out} = CPU Internal frequency

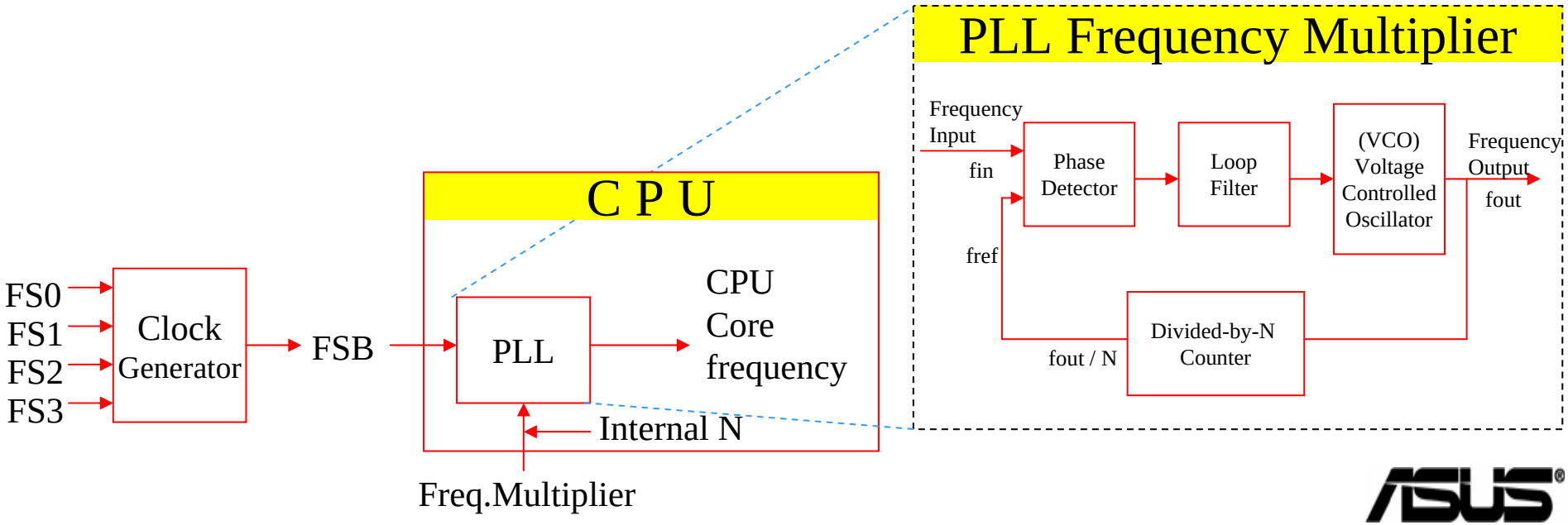
  $= N * f_{in}$



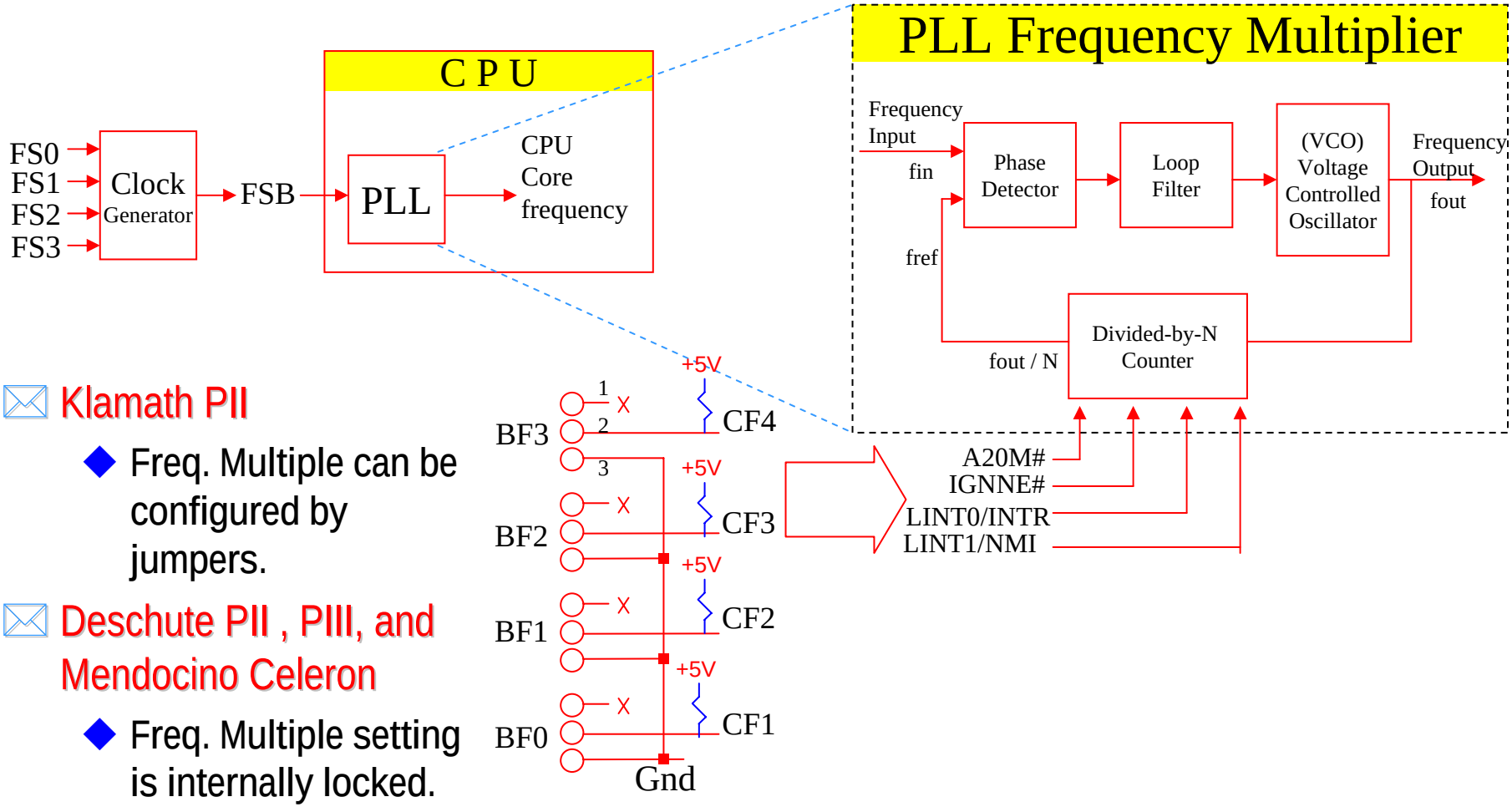
CPU FSB Frequency

- fin = FSB (Front Side Bus) frequency
  N = Frequency Multiplier setting

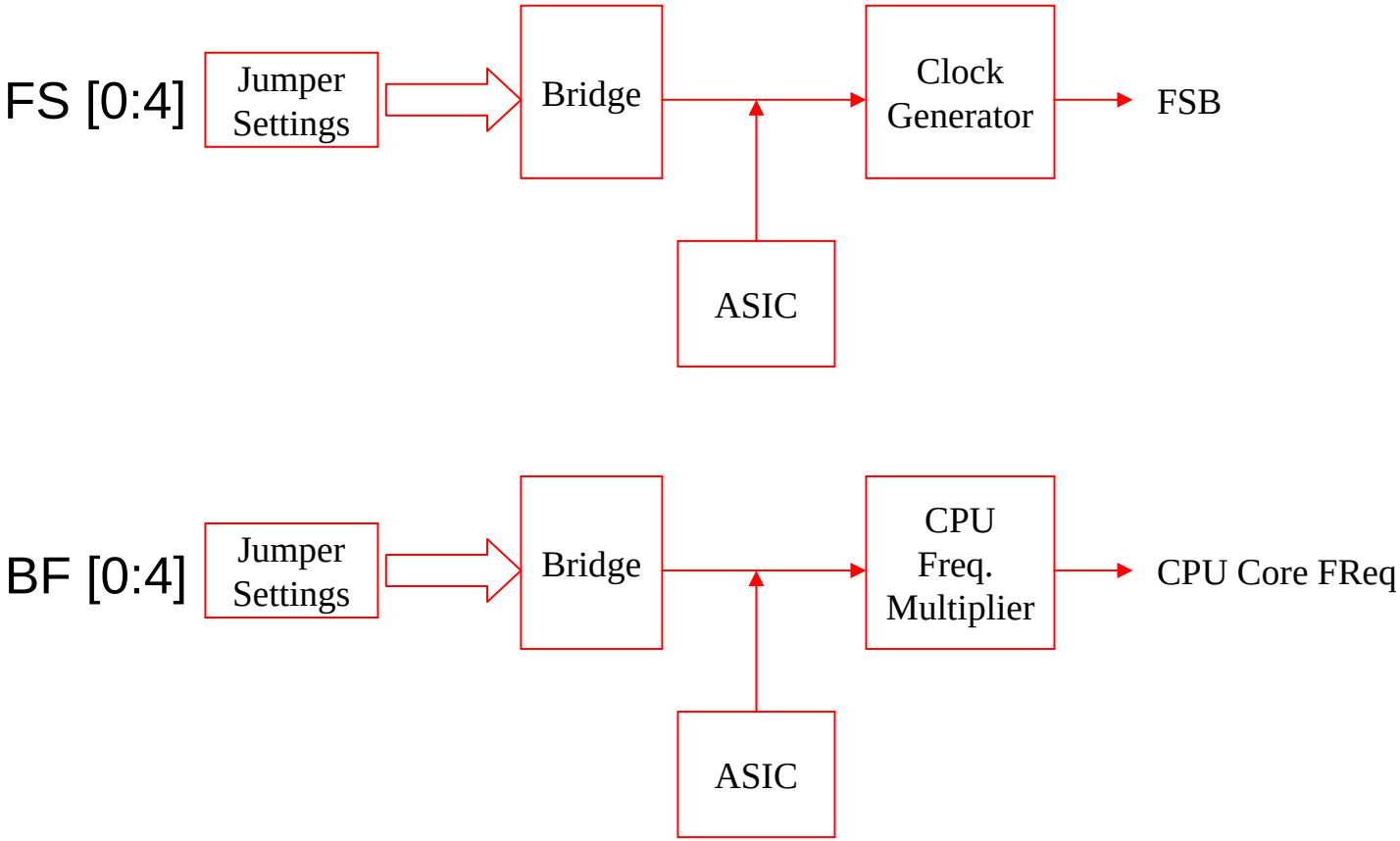
- fout = CPU Internal Core Frequency
  = N * fin



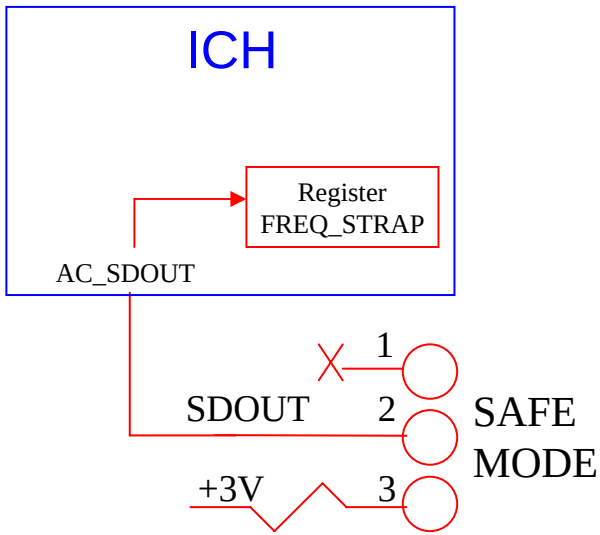
CPU Frequency Multiplier



- **Klamath PII**
  - Freq. Multiple can be configured by jumpers.
- **Deschute PII , PIII, and Mendocino Celeron**
  - Freq. Multiple setting is internally locked.
- **Engineering Sample**
  - Freq. Multiple still can be configured.


FS [0:4]
Jumper Settings
Bridge
Clock Generator
FSB
ASIC
BF [0:4]
Jumper Settings
Bridge
CPU Freq. Multiplier
CPU Core FReq
ASIC

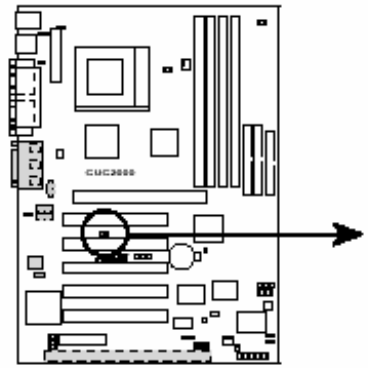
SAFE Mode Setting

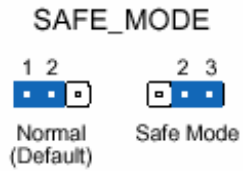


3) Safe Mode Setting (SAFE_MODE)

Usually processors have locked frequency multiples. In this case, there is no way to exceed the specified multiple whether through motherboard settings or BIOS setup. With unlocked processors, exceeding the specified multiple is possible through BIOS setup. Exceeding the specified multiple may result in hanging during bootup. If this occurs, enable *Safe Mode* to force a multiple of 2 and 100MHz FSB to enter BIOS setup to correct the problem.

Setting	SAFE_MODE
Normal	[1-2] (default)
Safe Mode	[2-3]

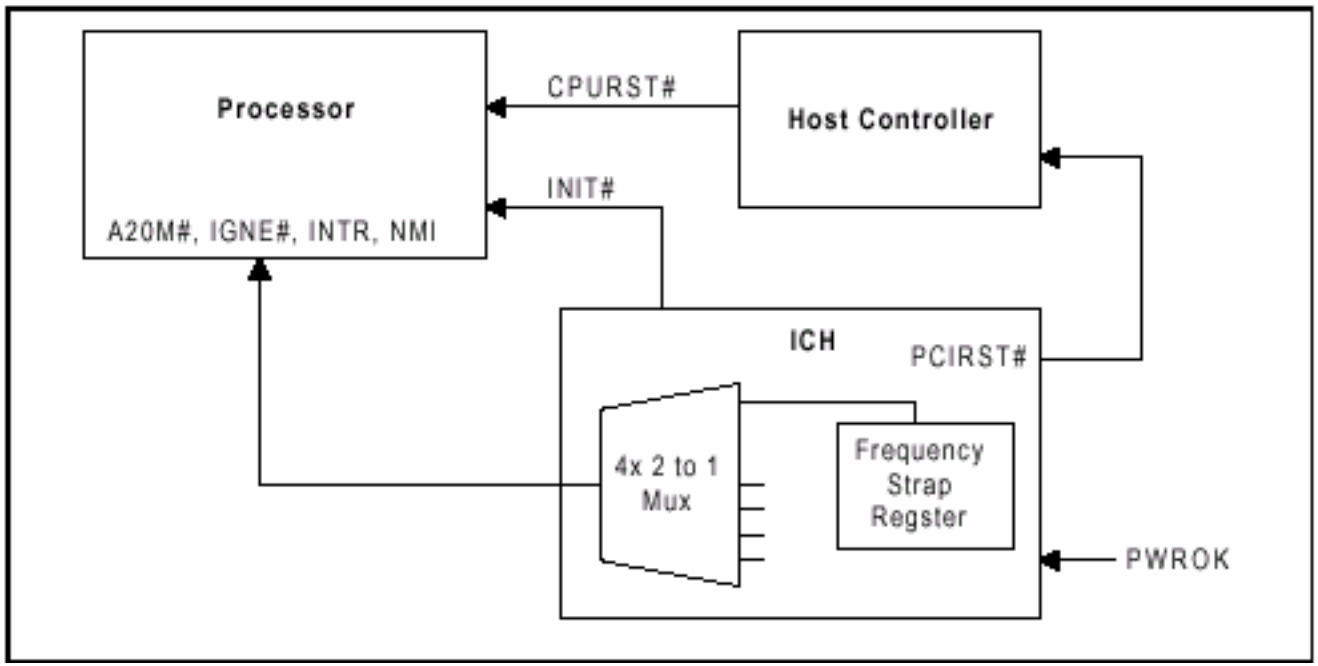




CUC2000 Safe Mode Setting

SAFE Mode Setting

ICH Signal Strapping



[BF 0,1,2,3]
= [H, H, H, H]

===> X 2

FREQ_STRAP bits [3:0]	Sets High/Low level for corresponding signal
3	NMI
2	INTR
1	IGNNE#
0	A20M#

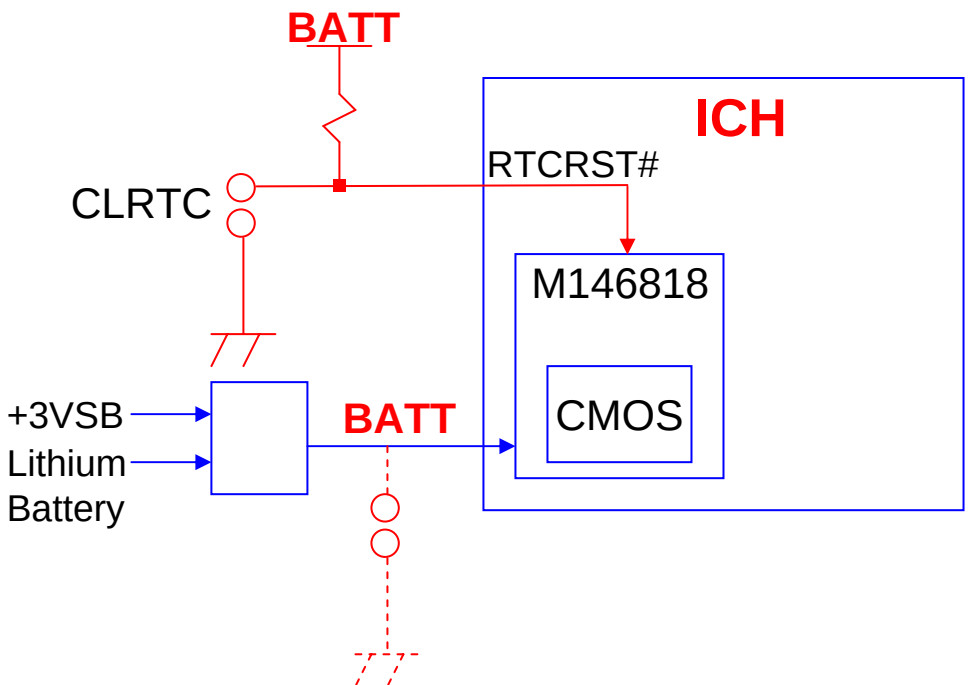
NOTE: The FREQ_STRAP register is in the RTC well. The value in the register can be forced to 1111h via a pinstrap (AC_SDOUT signal), or the ICH can automatically force the speed strapping to 1111h if the processor fails to boot.

Functions activated in G3 state

- Functions in G3 state being maintained on board by the BATT power are :
  - CMOS SRAM (in ICH)
  - RTC (Real Time Clock) (in ICH)
  - AC Power Loss Restart (in ICH)
  - New CPU Detection (On board)
  - Chassis Intrusion (On board)

CMOS

- Motorola 146818 RTC chip
  - 256-Byte CMOS Memory (SRAM) powered by BATT
  - PIIX4 allows the short-ckt of BATT to clear CMOS.
  - ICH prefers the RTCRST# to clear CMOS
- CMOS
  - POST = Power On Self Test



CPU

Post Code C5
Copy the BIOS from Flash ROM into E000-FFFF shadow DRAM so that POST will go faster

Post Code 0B
Read CMOS Data into BIOS Stack Area

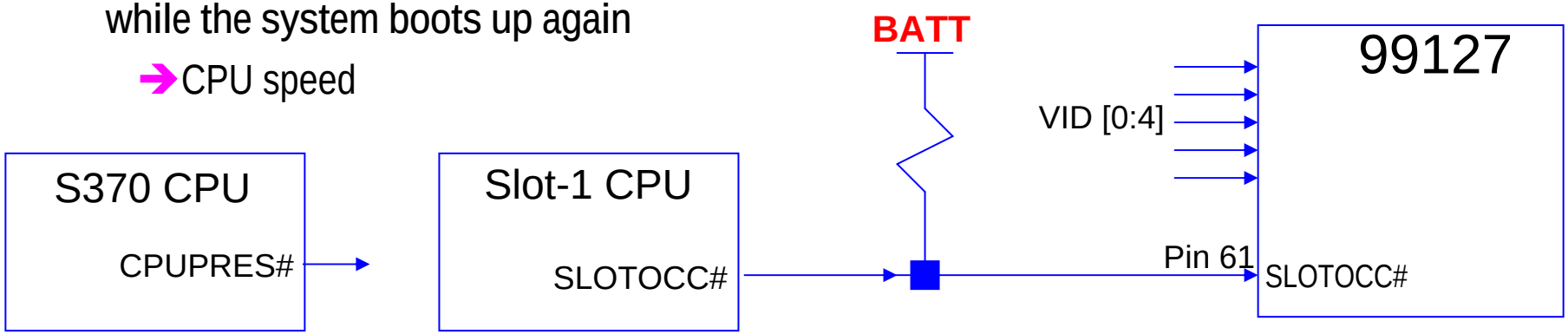
GO ON the POST procedure

CPU Presence Detection

- Slot-1 CPU
  - SLOTOCC# = Slot Occupation
- S370 CPU
  - CPUPRES# = CPU Presence
- This function is powered by Lithium battery
  - BATT
  - Still working in G3 state
- Any action of removing the CPU
  - will cause the BIOS to configure CPU again while the system boots up again
    - ➔CPU speed

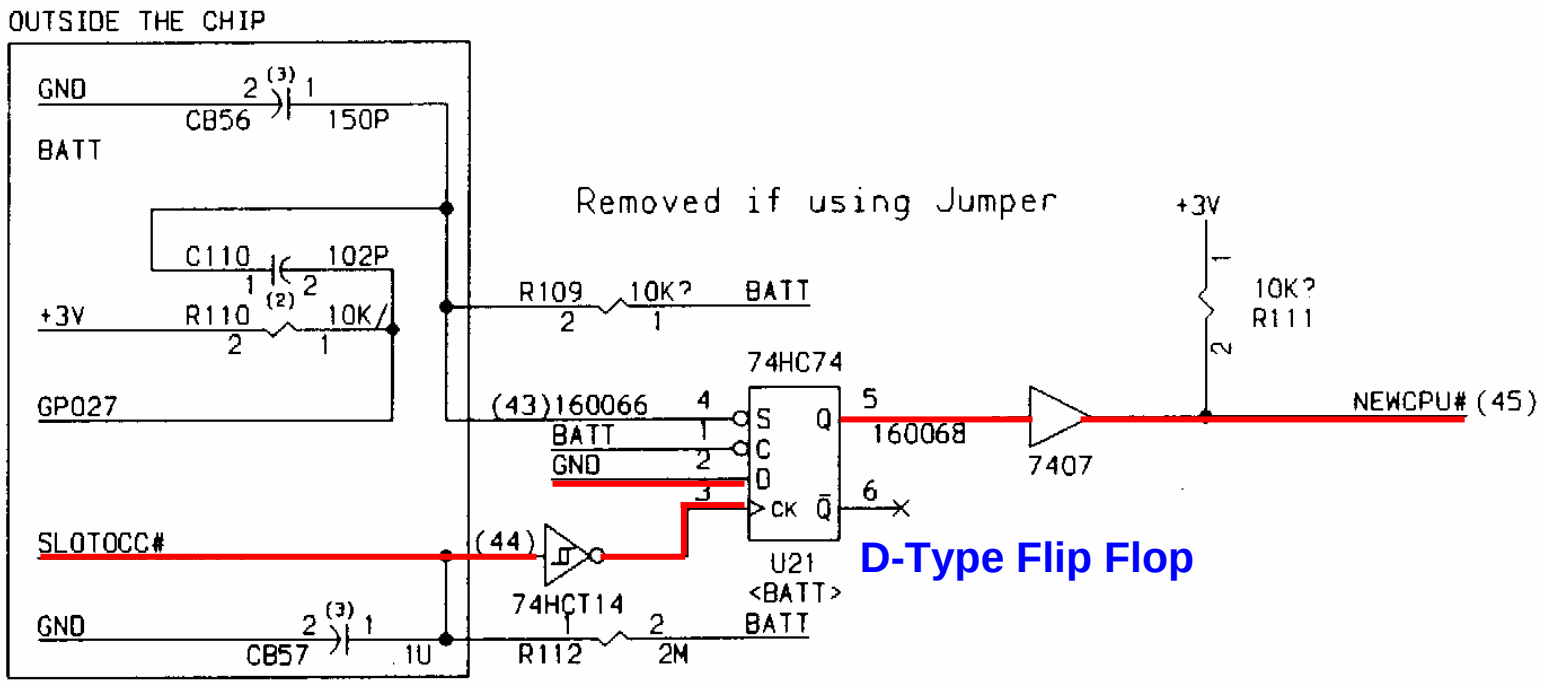
Table 32. Slot 1 Occupation Truth Table

Signal	Value	Status
SLOTOCC# VID[4:0]	0 Anything other than '11111'	Processor with core in Slot 1 connector.
SLOTOCC# VID[4:0]	0 11111	Terminator cartridge in Slot 1 connector (i.e., no core present).
SLOTOCC# VID[4:0]	1 Any value	Slot 1 connector not occupied.



CPU Presence Detection

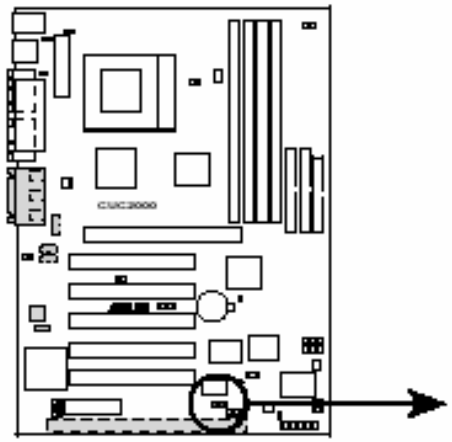
ASUS ASIC 97127



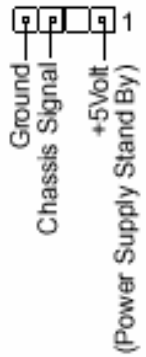
Chassis Intrusion

8) Chassis Intrusion Lead (4-1 pin CHASSIS)

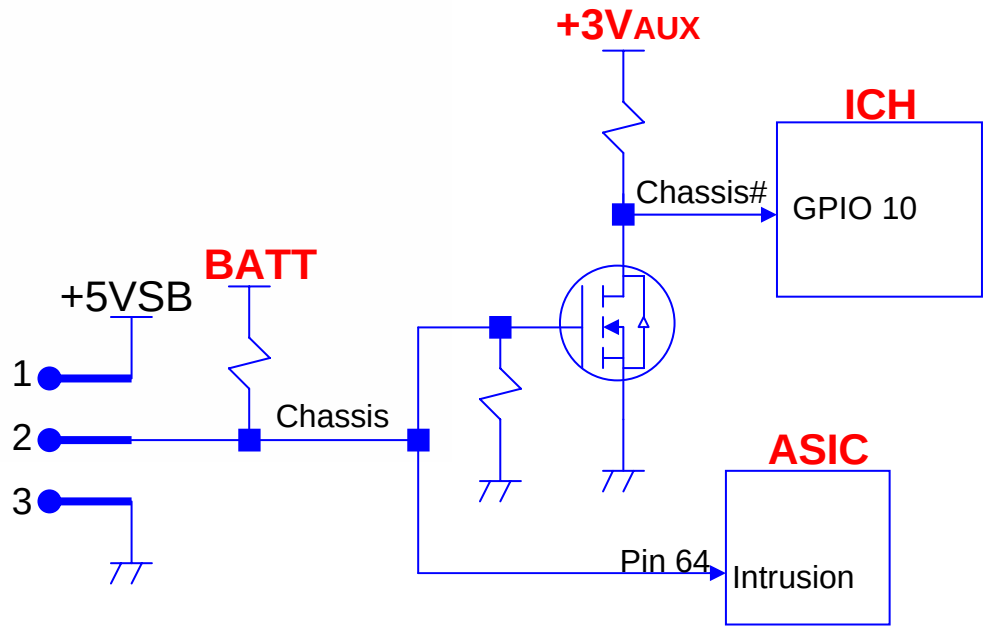
This requires an external detection mechanism such as a chassis intrusion monitor/sensor or microswitch. The sensor is triggered when a high level signal is sent to the Chassis Signal lead, which occurs when a panel switch or light detector is triggered. This function requires the optional ASUS CIDB chassis intrusion module to be installed (see *7. APPENDIX*). If the chassis intrusion lead is not used, a jumper cap must be placed over the pins to close the circuit.



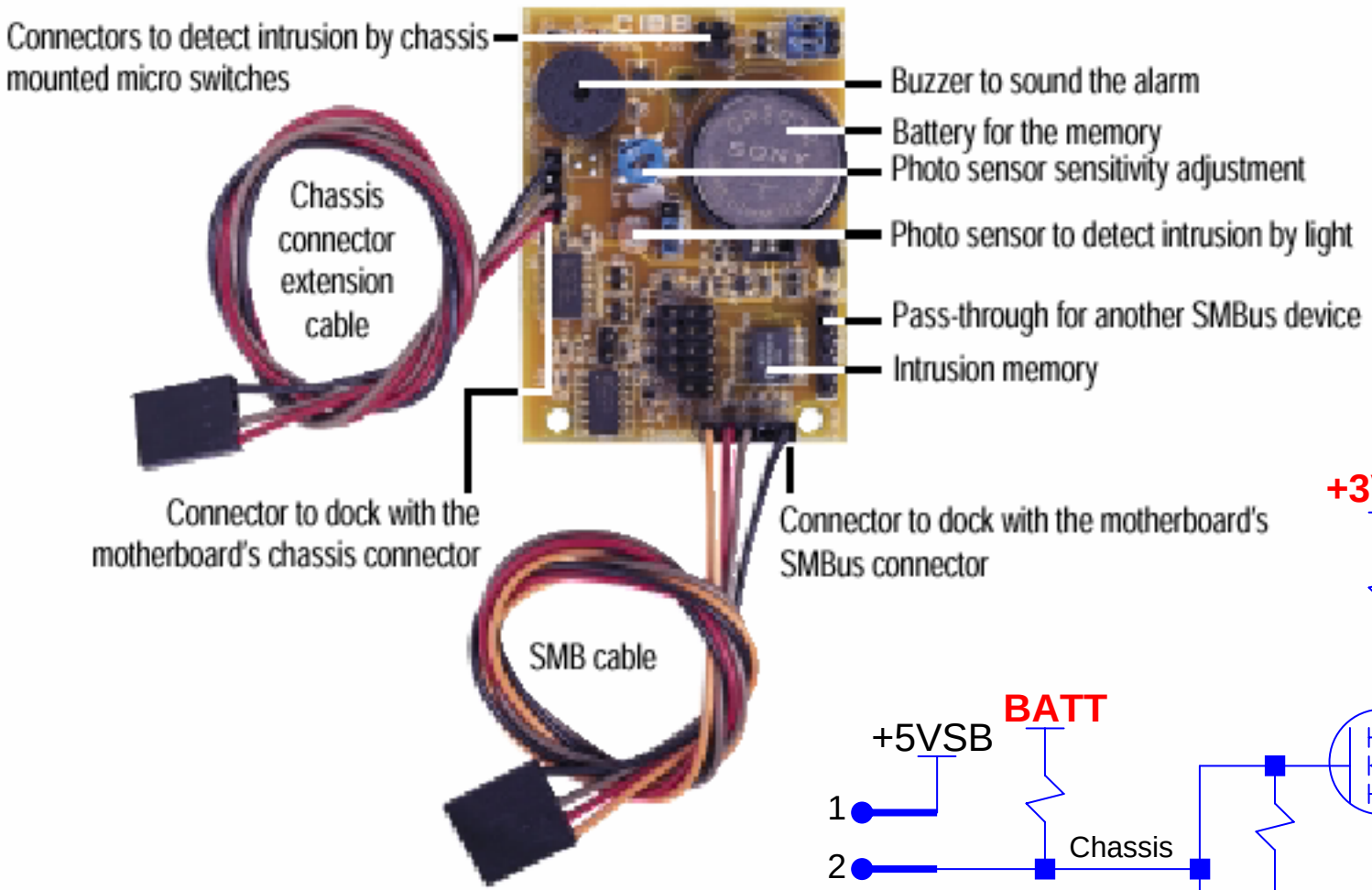
CHASSIS

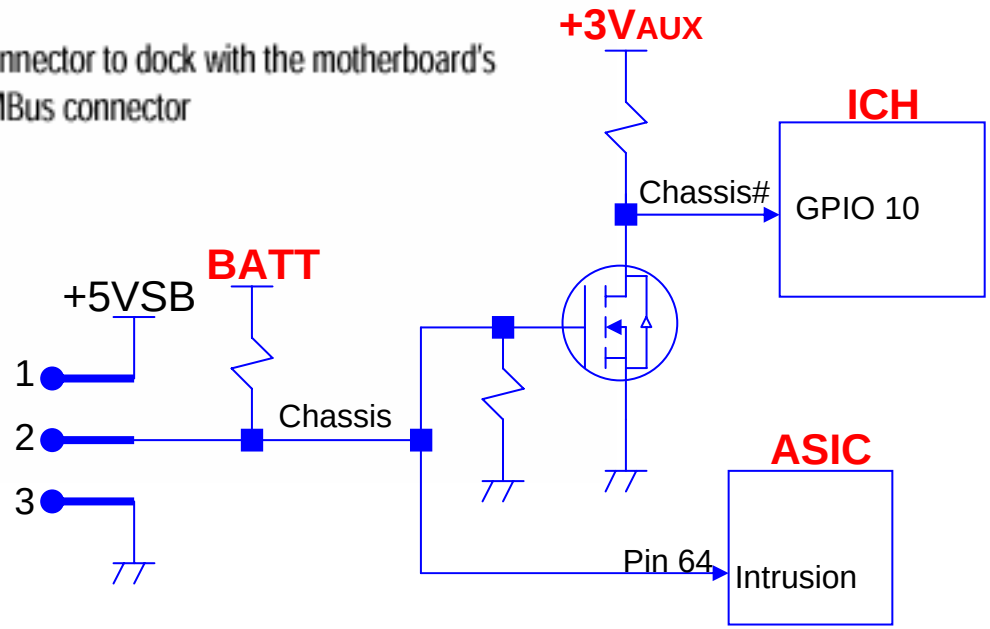


CUC2000 Chassis Open Alarm Lead



Chassis Intrusion





3. Wake On LAN

Wake On Ring

Wake Up By KB

Wake On USB

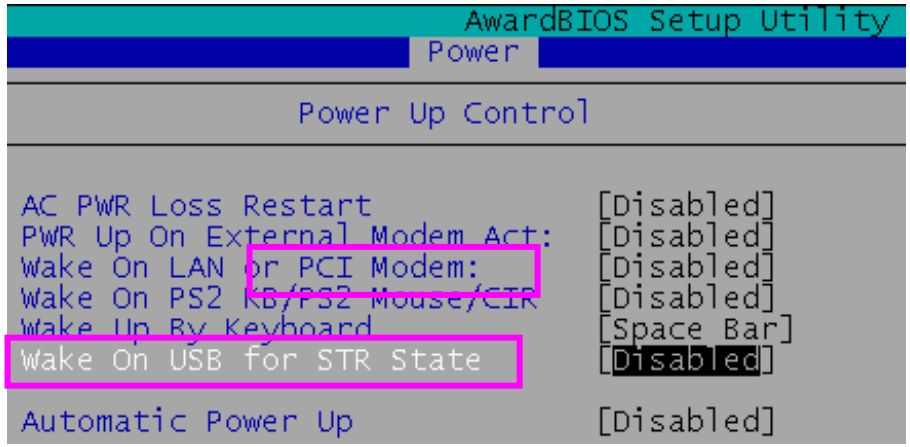
AC Power Loss Restart

POWER UP CONTROL

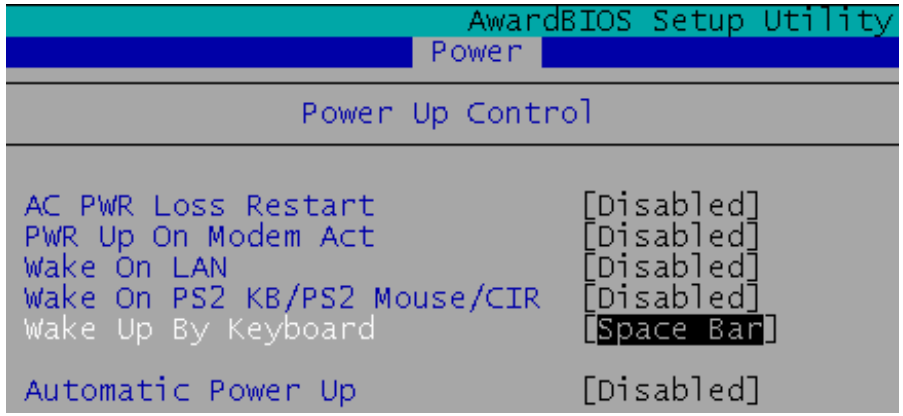
BIOS Setup \ Power \ Power Up Control

- AC Power Loss Restart
- PWR Up On external Modem Act
- Wake On LAN or PCI Modem card
- Wake On PS/2 KB / PS2 Mouse
- Wake Up By Keyboard
- Wake On USB Device
- Automatic Power Up

CUC2000, CUWE-FX



P3B-F, P3WE



ICH : Wake Up Events

Causes of Wake Events

Cause	States Can Wake From	How Enabled
RTC Alarm	S1 - S5 (Note 2)	Set RTC_EN bit in PM1_EN Register
Power Button	S1 - S5 (Note 1)	Always enabled as Wake event
GPI[0:n]	S1 - S5 (Note 2)	GPE1_EN register
V USB	S1 - S4	Set USB_EN bit in GPE0_EN Register
RI#	S1 - S5 (Note 2)	Set RI_EN bit in GPE0_EN Register
V AC97	S1 - S4	Set AC97_EN bit in GPE0_EN Register
PME#	S1 - S5 (Note 2)	Set PME_EN bit in GPE0_EN Register.
V SMBALERT#	S1 - S4	SMB_WAK_EN in the GPE0 Register

ACPI signaling of ICH

- The ICH directly supports different sleep states (S1-S5), which are entered by setting the SLP_EN bit, or due to a Power Button Override.
- Sleep states are initiated by
  - Setting the desired type in the SLP_TYP field and setting the SLP_EN bit.

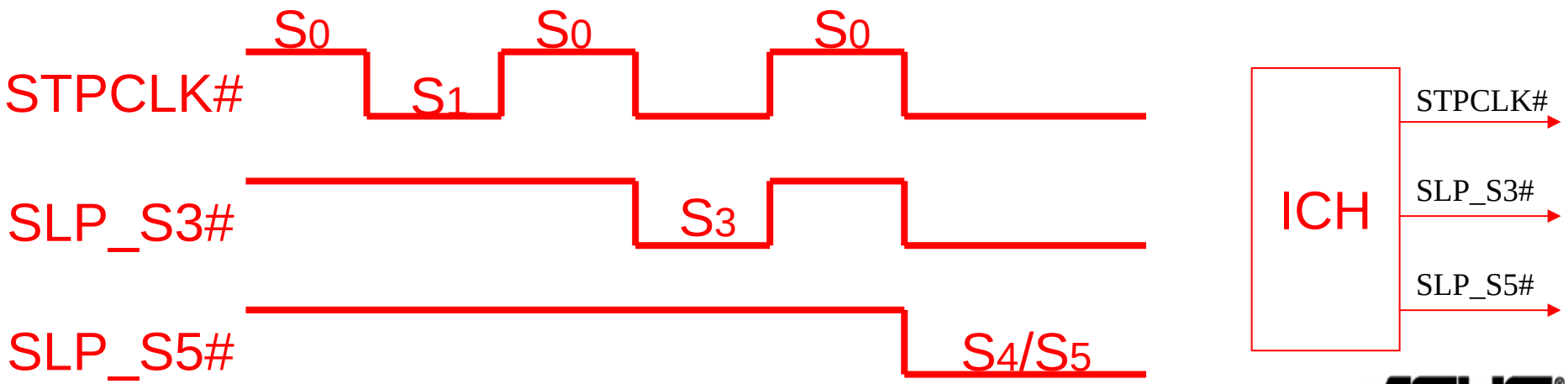
PM1_CNT—Power Management 1 Control

Bit	Description
13	**SLP_EN — WO.** This is a write-only bit and reads to it always return a zero. 1 = Setting this bit causes the system to sequence into the Sleep state defined by the SLP_TYP field.
12:10	**SLP_TYP.** This 3-bit field defines the type of Sleep the system should enter when the SLP_EN bit is set to 1. 000 = ON 001 = Just assert STPCLK#. Puts processor in Stop-Grant state. Also assert CPUSLP#, to put processor in sleep state. 010 = Reserved 011 = Reserved 100 = Reserved 101 = Suspend-To-RAM. Assert SLP_S3#. 110 = Suspend-To-Disk. Assert SLP_S3# and , SLP_S5#. 111 = Soft Off. Assert SLP_S3#, and SLP_S5#

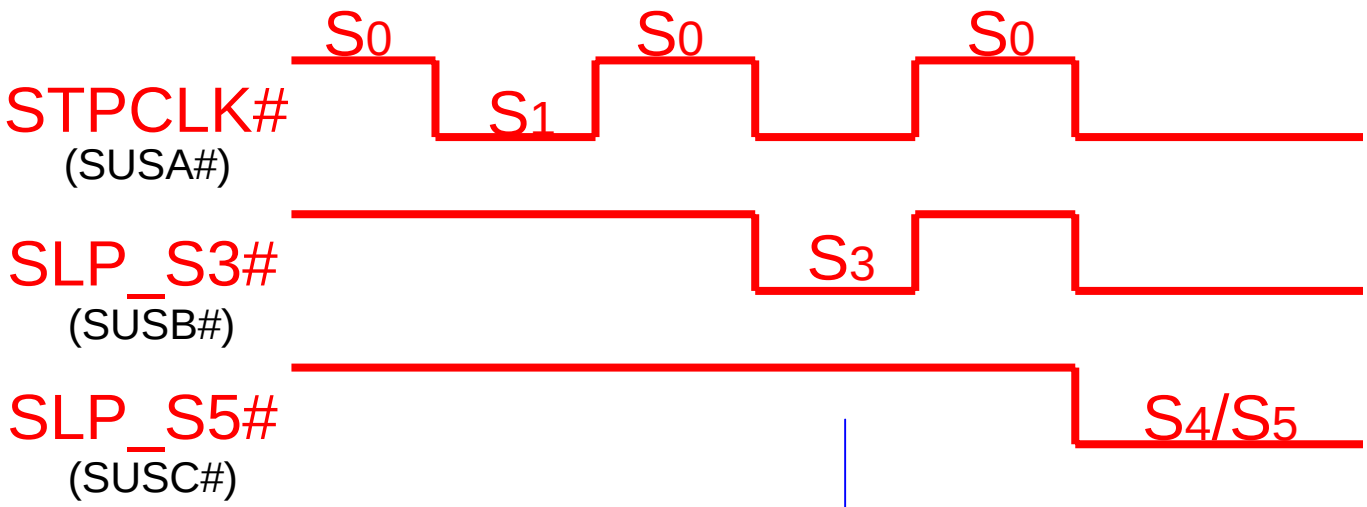
ACPI signaling of ICH

Sleep Types

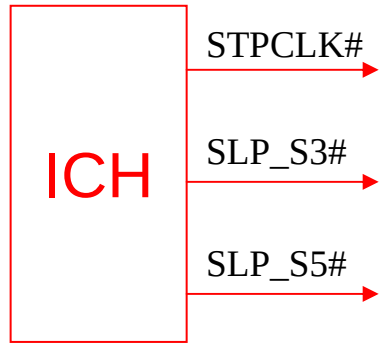
Sleep Type	Comment
S1	ICH asserts the processor SLP# signal. This will lower the processor's power consumption. No snooping is possible in this state.
S2	Not supported.
S3	ICH asserts SLP_S3#. The SLP_S3# signal will control the power to non-critical circuits. Power will only be retained to devices needed to wake from this sleeping state, as well as to the memory.
S4	ICH asserts SLP_S3# and SLP_S5#. The SLP_S5# will shut off the power to the memory subsystem. Only devices needed to wake from this state should be powered.
S5	Same as S4. ICH asserts SLP_S3# and SLP_S5#. The SLP_S5# signal will shut off the power to the memory subsystem. Only devices needed to wake from this state should be powered.

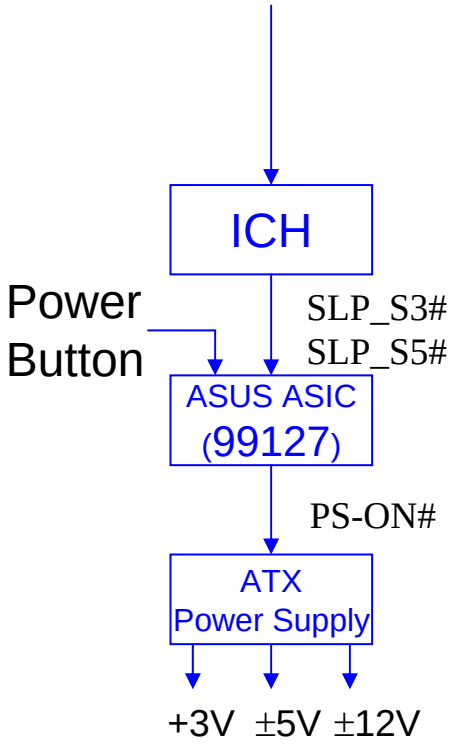


ACPI signaling of ICH



(SUSA,B,C# are forPIIX4)

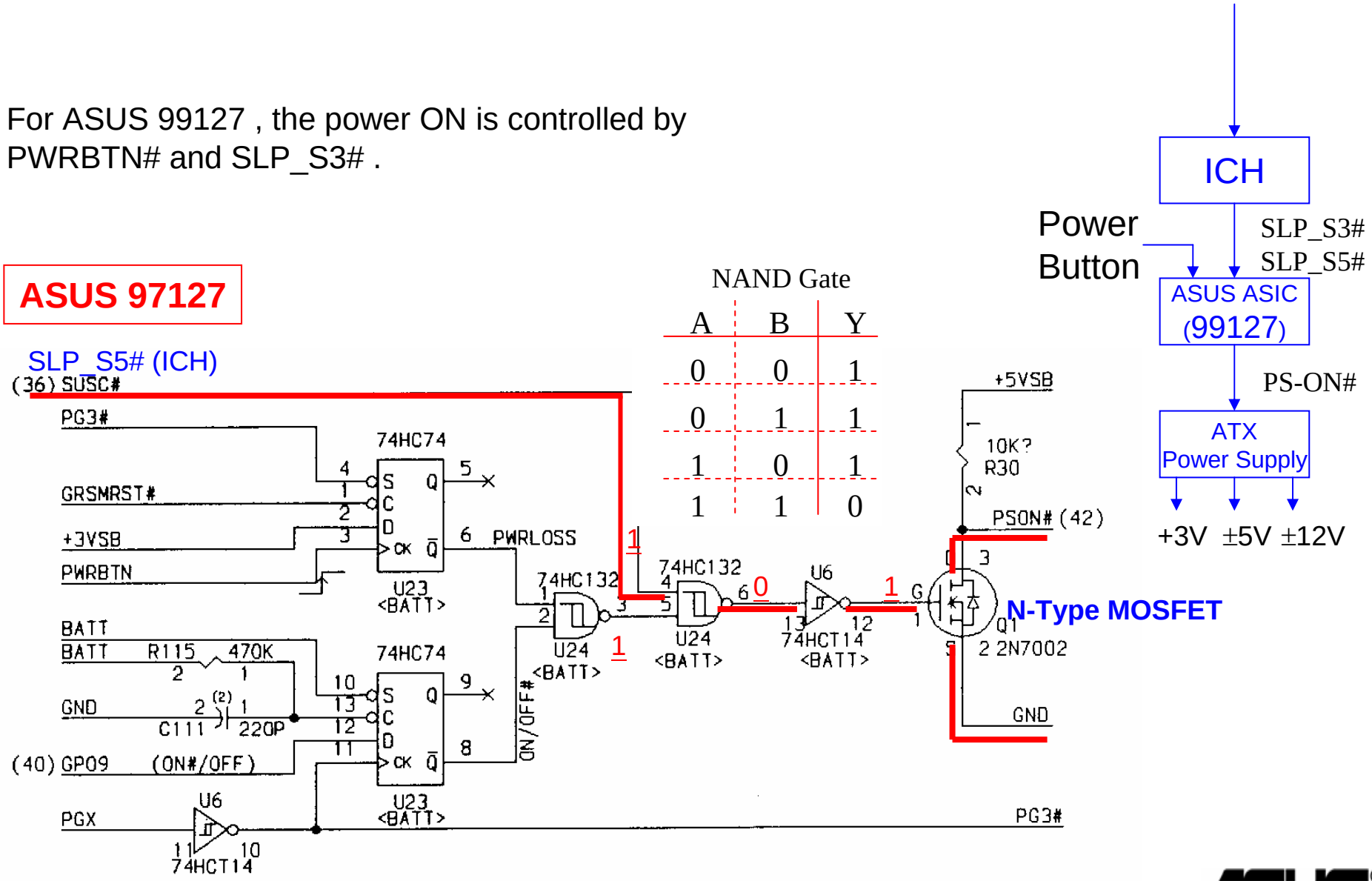




ACPI signaling of ICH

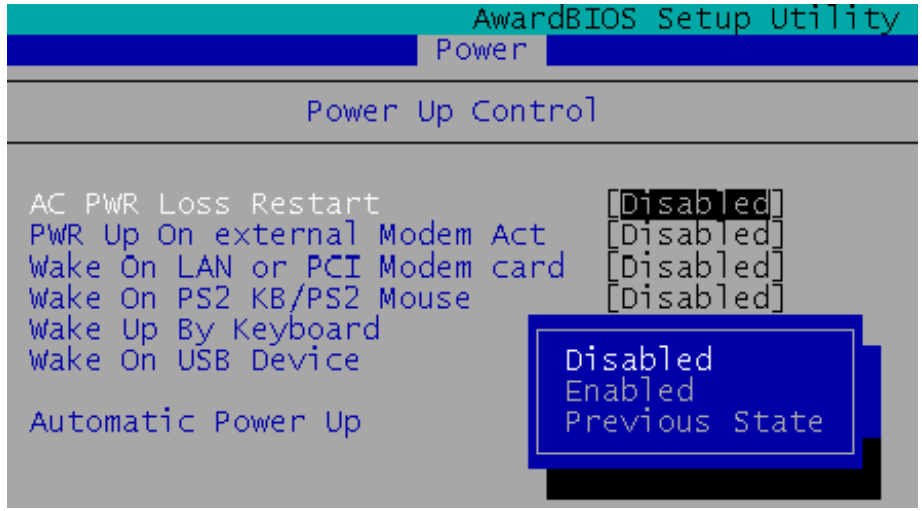
For ASUS 99127 , the power ON is controlled by PWRBTN# and SLP_S3# .

ASUS 97127



AC Power Loss Restart

BIOS setting		State of AC Power Loss	Setting of AC Power Loss Restart		
WOL	WOR		Previous	Disabled	Enabled
Disable	Disable	S5 (Soft Off)	OFF	OFF	ON
Disable	Disable	S0 (Working)	ON	OFF	ON
Disable	Enable	S5 (Soft Off)	ON→OFF	ON→OFF	ON
Disable	Enable	S0 (Working)	ON	ON→OFF	ON
Enable	Disable	S5 (Soft Off)	ON→OFF	ON→OFF	ON
Enable	Disable	S0 (Working)	ON	ON→OFF	ON
Enable	Enable	S5 (Soft Off)	ON→OFF	ON→OFF	ON
Enable	Enable	S0 (Working)	ON	ON→OFF	ON



AC Power Loss

1. The AC power cord was unplugged from the ATX power supply
2. The AC power was lost

AC Power Loss Restart

- the AC Power is back
- +5V standby and the resulting standby power is back
- determine if the system would be back to original S0 state or stay in S5 state

ICH : AfterG3_En bit

BIOS setting		State of AC Power Loss	Setting of AC Power Loss Restart		
WOL	WOR		Previous	Disabled	Enabled
Disable	Disable	S5 (Soft Off)	OFF	OFF	ON
Disable	Disable	S0 (Working)	ON	OFF	ON
Disable	Enable	S5 (Soft Off)	ON→OFF	ON→OFF	ON
Disable	Enable	S0 (Working)	ON	ON→OFF	ON
Enable	Disable	S5 (Soft Off)	ON→OFF	ON→OFF	ON
Enable	Disable	S0 (Working)	ON	ON→OFF	ON
Enable	Enable	S5 (Soft Off)	ON→OFF	ON→OFF	ON
Enable	Enable	S0 (Working)	ON	ON→OFF	ON

- ON
  - Return to S0
- OFF
  - Remain in S5
- ON → OFF
  - CPU is turned on for a while to configure the wake-up circuits of WOL, WOR, etc.

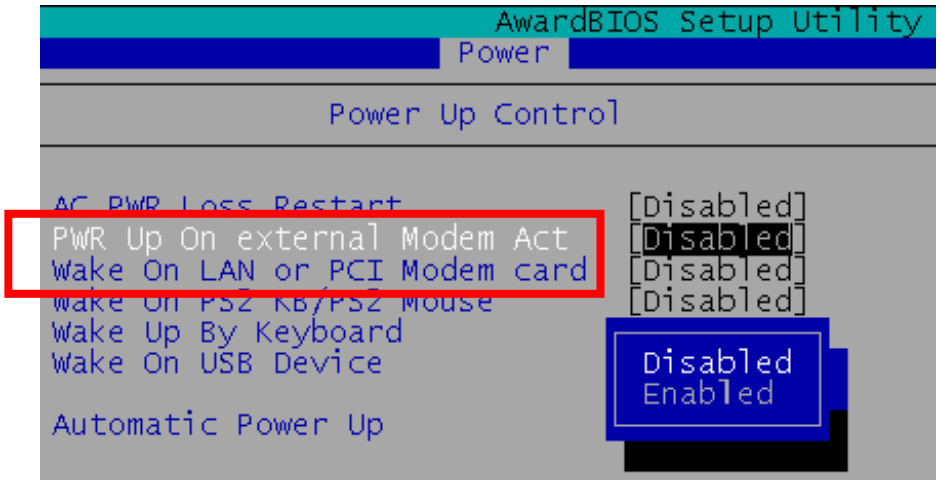
Transitions Due To Power Failure

State at Power Failure	AFTERG3_EN bit	Transition When Power Returns
S0	1 0	S5 S0
S1	1 0	S5 S0
S3	1 0	S5 S0
S4	1 0	S4 S0

GEN_PMCON_3—General PM Configuration 3 Register (PM—D31:F0)

Bit	Description
0	**AFTERG3_EN:** Determines what state to go to when power is re-applied after a power failure (G3 state). In the S5 state, the only enabled wake event is the Power Button or any enabled wake event that was preserved through the power failure. This bit is in the RTC well and is not cleared by any type of reset except writes to CF9h or RTCRST#. 0 = System will return to S0 state (boot) after power is re-applied. 1 = System will return to the S5 state (except if it was in S4, in which case it will return to S4).

WOR



WOR

- Wake On Ring
- RI# : Ring-Indicate signal is generated by modem to inform the system an incoming call.

PWR Up On Modem Act [Disabled]

This allows either settings of [Enabled] or [Disabled] for powering up the computer when the modem receives a call while the computer is in Soft-off mode. **NOTE:** The computer cannot receive or transmit data until the computer and applications are fully running. Thus connection cannot be made on the first try. Turning an external modem off and then back on while the computer is off causes an initialization string that will also cause the system to power on. Configuration options: [Disabled] [Enabled]

Modem

1. External Modem
2. Internal Modem Card

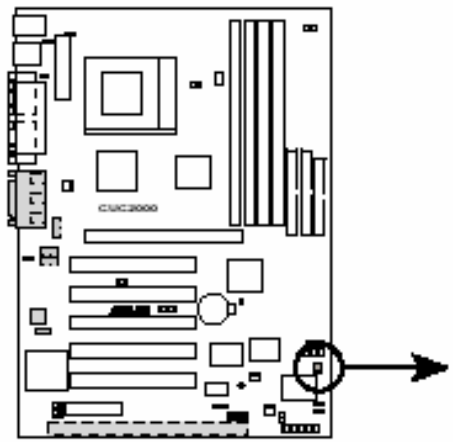
Wake On Ring

Internal Modem card

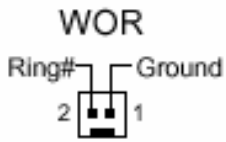
12) Wake-On-Ring Connector (2-pin WOR)

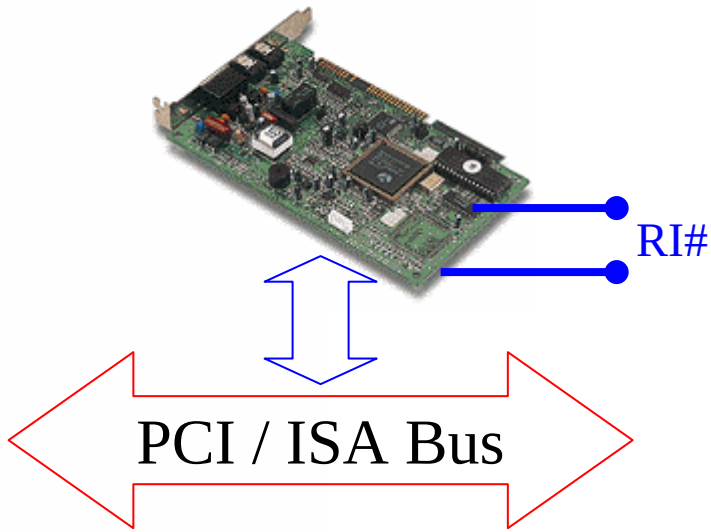
This connector connects to internal modem cards with a Wake-On-Ring output. The connector powers up the system when a ringup packet or signal is received through the internal modem card. **NOTE:** For external modems, Wake-On-Ring is detected through the COM port.

IMPORTANT: This feature requires that **Wake-On-Ring** features are enabled (see ***4.4.3 Power Management***) and that your system has an ATX power supply with at least 720mA +5V standby power.



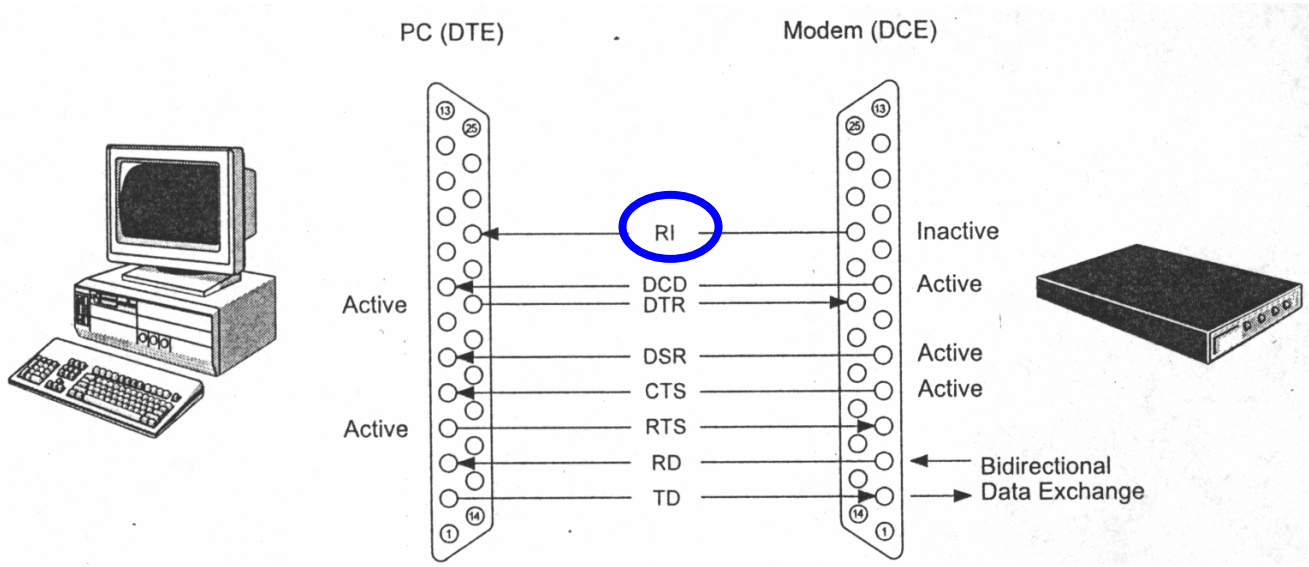
CUC2000 Wake-On-Ring Connector

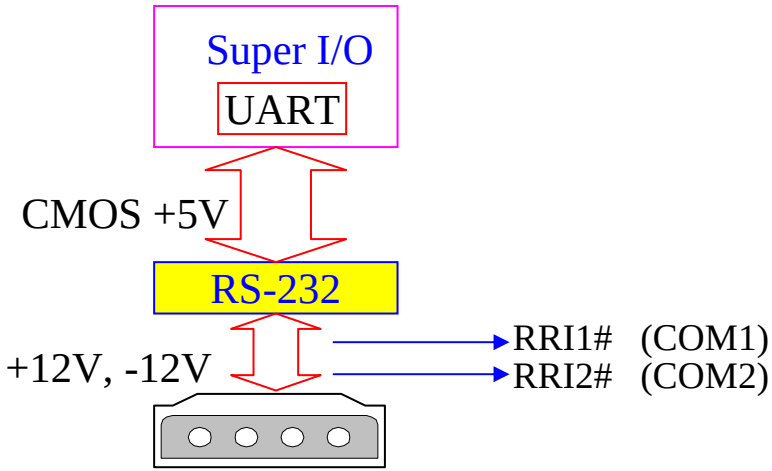




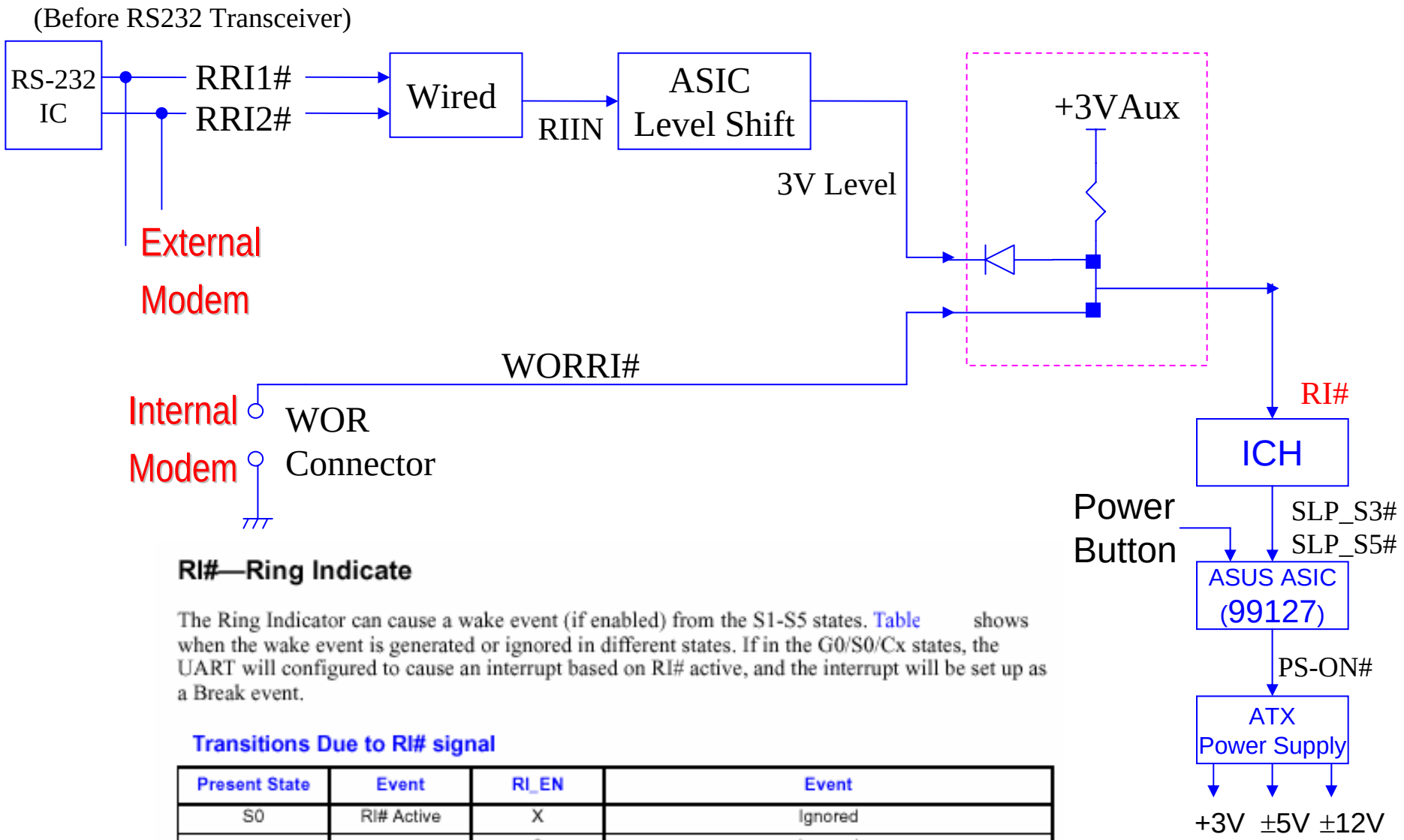
WOR

External Modem





WOR



RI#—Ring Indicate

The Ring Indicator can cause a wake event (if enabled) from the S1-S5 states. Table shows when the wake event is generated or ignored in different states. If in the G0/S0/Cx states, the UART will configured to cause an interrupt based on RI# active, and the interrupt will be set up as a Break event.

Transitions Due to RI# signal

Present State	Event	RI_EN	Event
S0	RI# Active	X	Ignored
S1-S5	RI# Active	0	Ignored
		1	Wake Event

Filtering/Debounce on RI# will not be done in ICH. Can be in modem or external.

WOR (ICH)

GPE0_STS—General Purpose Event 0 Status Register

Note: This register is symmetrical to the General Purpose Event 0 Enable Register. If the corresponding _EN bit is set, then when the _STS bit get set, the ICH generates a Wake Event. Once back in an S0 state (or if already in an S0 state when the event occurs), the ICH will also generate an SCI if the SCI_EN bit is set, or an SMI# if the SCI_EN bit is not set. No SCI/SMI# or wake event on THRMOR_STS since no corresponding _EN bit. None of these bits should be reset by CF9h write. All should be reset by RSMRST#, except for RI_STS.

Bit	Description
8	**RI_STS.** 1 = This bit is set to 1 by hardware when the RI# input signal goes active. The value of this bit must be maintained, even through a G3 state. 0 = This bit can be reset by writing a one to this bit position. **NOTE:** This bit is not effected by a hard reset caused by a CF9h write.

GPE0_EN—General Purpose Event 0 Enables Register

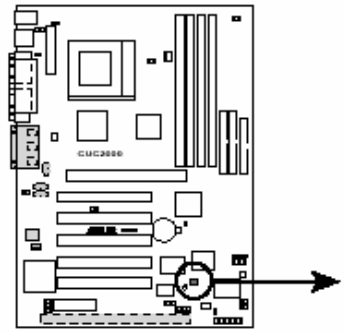
Bit	Description
8	**RI_EN.** When both RI_EN and RI_STS are set, a Wake event will occur. If RI_EN is not set, then when RI_STS is set, no Wake event will occur. This bit is only cleared by software or RTCRST#.

WOL

11) Wake-On-LAN Connector (3-pin WOL_CON)

This connector connects to a LAN card with a Wake-On-LAN output, such as the ASUS PCI-L101 Ethernet card (see ***7. Appendix***). The connector powers up the system when a wakeup packet or signal is received through the LAN card.

IMPORTANT: This feature requires that **Wake-On-LAN** features are enabled (see ***4.4.3 Power Management***) and that your system has an ATX power supply with at least 720mA +5V standby power.



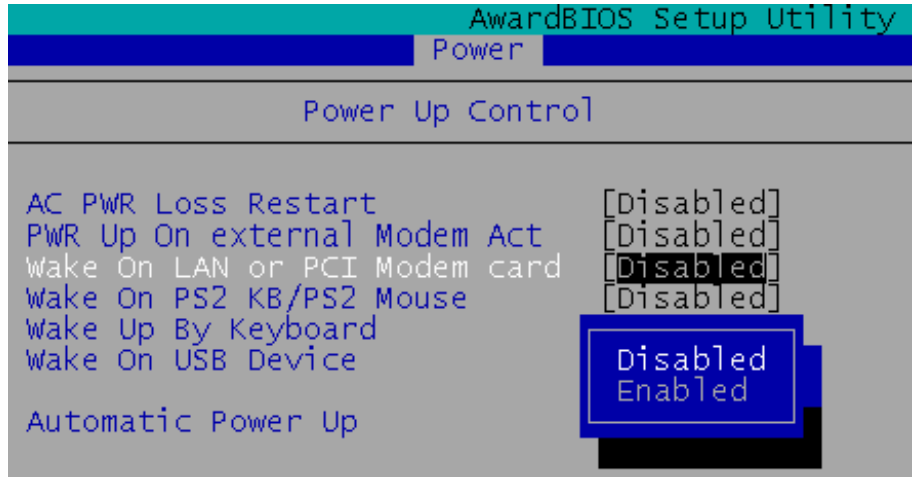
CUC2000 Wake-On-LAN Connector

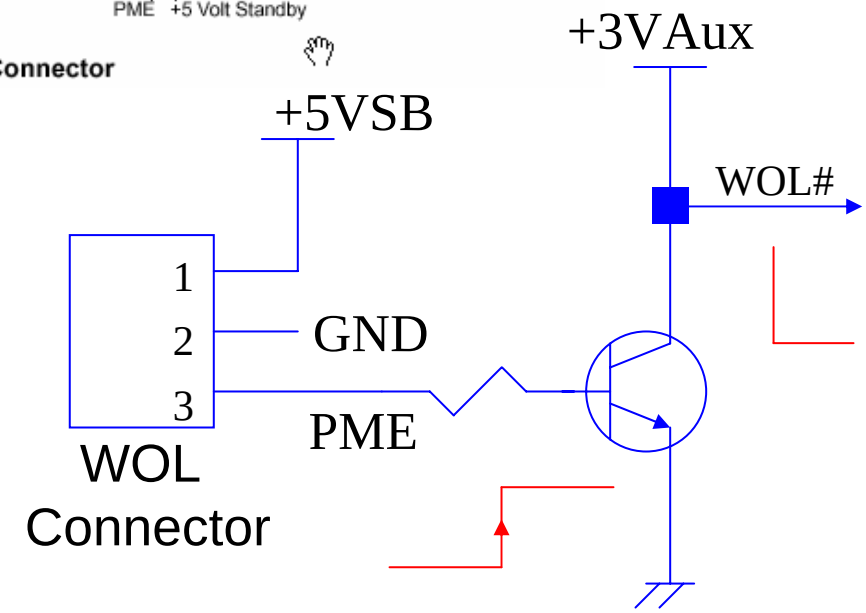
IMPORTANT: Requires an ATX power supply with at least 720mA +5 volt standby power

WOL_CON

Ground

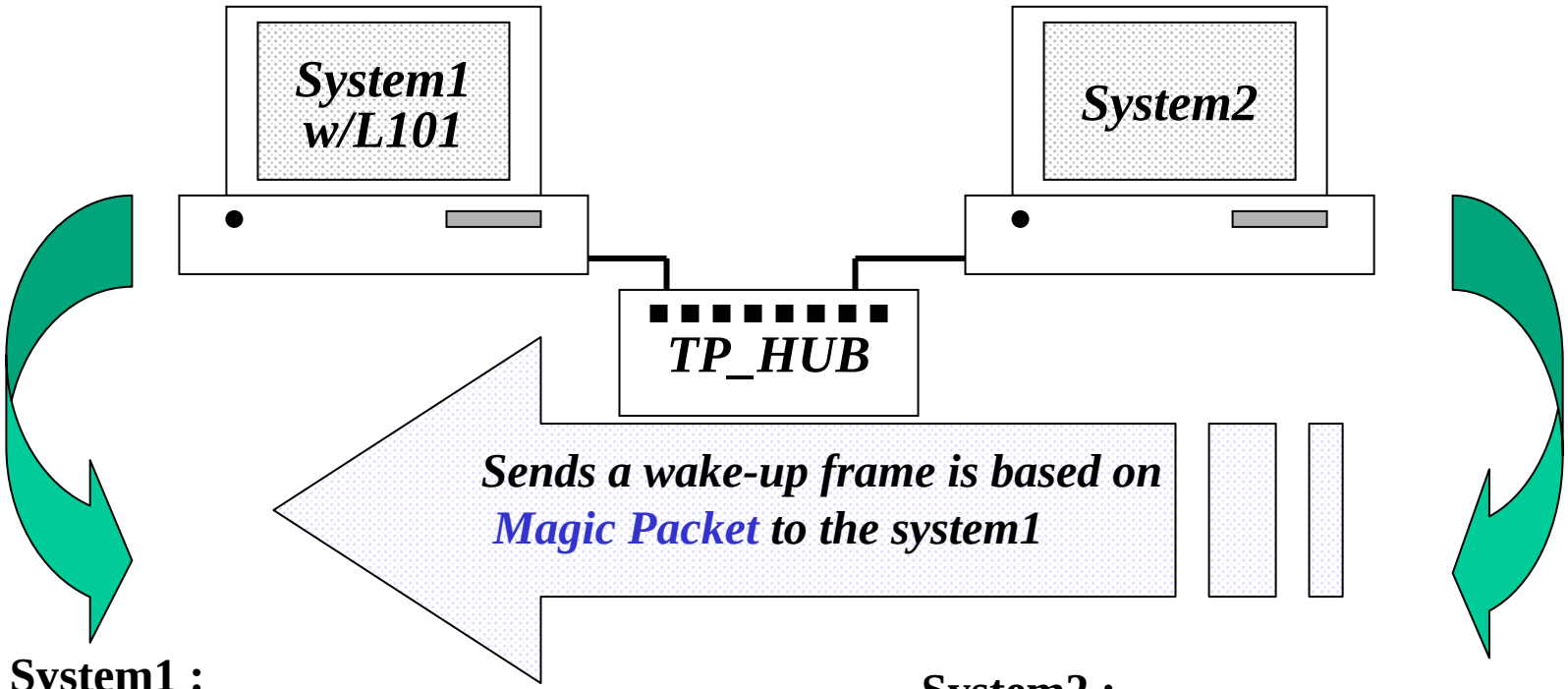
PME +5 Volt Standby





WOL

How Wake on LAN works?



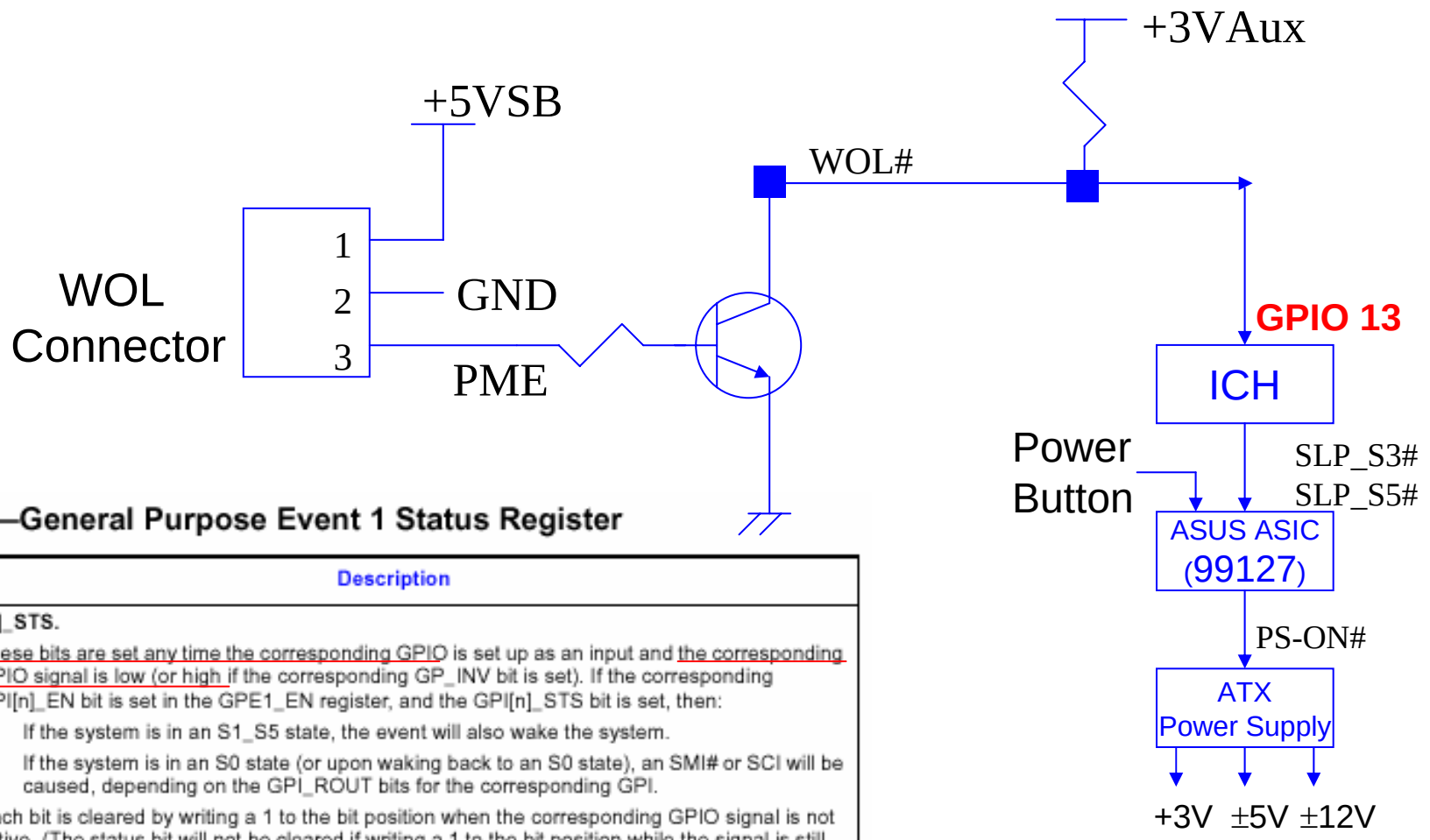
System1 :

1. Remote network management s/w for client (Intel's LANDesk s/w)
2. Enable System BIOS WOL
3. Receives & analyzes media access control (MAC) address
4. The client is turned on.

System2 :

1. Remote network management s/w for server (Intel's LANDesk s/w)
2. Send wake-up frame

WOL



GPE1_STS—General Purpose Event 1 Status Register

Bit	Description
15:0	**GPI[n]_STS.** 1 = These bits are set any time the corresponding GPIO is set up as an input and the corresponding GPIO signal is low (or high if the corresponding GP_INV bit is set). If the corresponding GPI[n]_EN bit is set in the GPE1_EN register, and the GPI[n]_STS bit is set, then: • If the system is in an S1_S5 state, the event will also wake the system. • If the system is in an S0 state (or upon waking back to an S0 state), an SMI# or SCI will be caused, depending on the GPI_ROUT bits for the corresponding GPI. 0 = Each bit is cleared by writing a 1 to the bit position when the corresponding GPIO signal is not active. (The status bit will not be cleared if writing a 1 to the bit position while the signal is still active).

GPE1_EN—General Purpose Event 1 Enable Register

Bit	Description
15:0	**GPI[n]_EN.** These bits enable the corresponding GPI[n]_STS bits being set to cause an SMI#, SCI, and/or wake event.

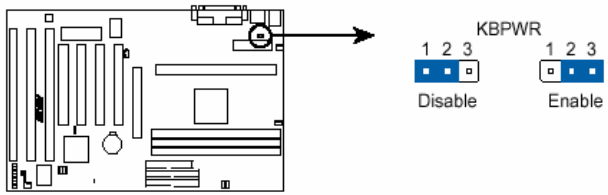
Wake Up By PS/2 KB

Wake On PS/2 KB

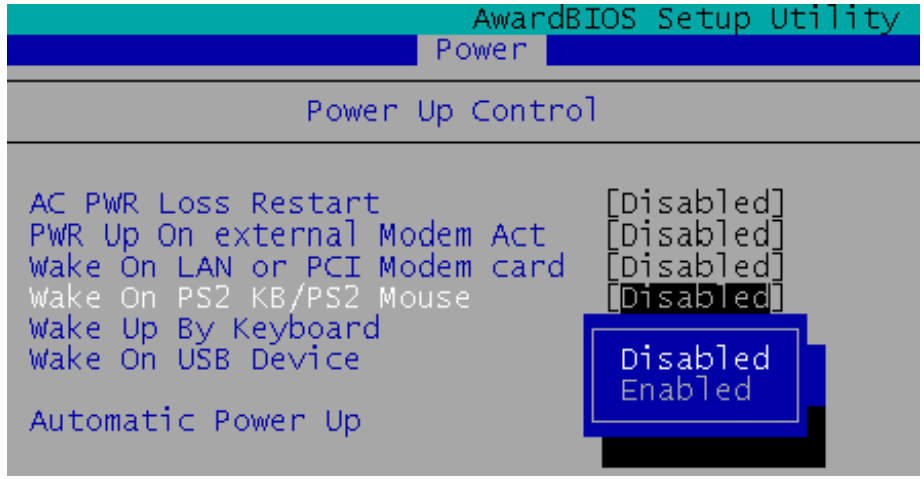
- +5VSB (ATX Srandby Power) is supplied to PS/2 ports by jumper setting

1. Keyboard Power Up (KBPWR)

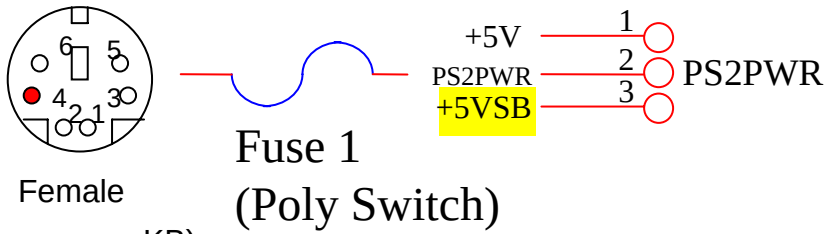
This allows you to disable or enable the keyboard power up function. Set to *Enable* if you want to use your keyboard (by pressing <Spacebar>) to power up your computer. This feature requires an ATX power supply that can supply at least 300mA on the +5VSB lead and the new ACPI BIOS support. The default is set to *Disable* because not all computers have the appropriate ATX power supply. Your computer will not function if you set this to *Enable* and if you do not have the right ATX power supply.



P2B Keyboard Power Up



1. Data
2. NC
3. GND
4. +5V
5. Clk
6. NC



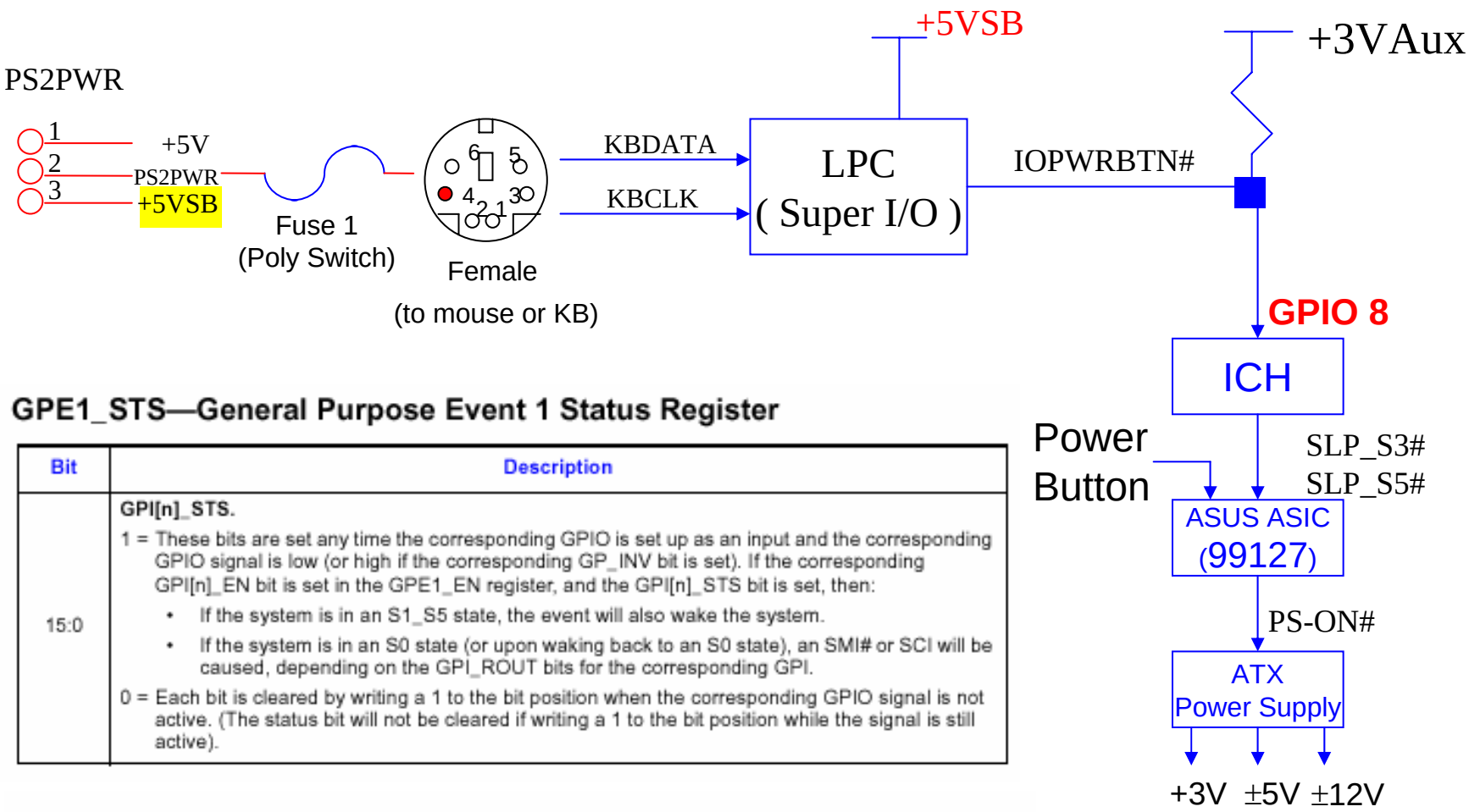
Female

(to mouse or KB)

Fuse 1

(Poly Switch)

Wake Up By PS/2 KB



GPE1_STS—General Purpose Event 1 Status Register

Bit	Description
15:0	**GPI[n]_STS.** 1 = These bits are set any time the corresponding GPIO is set up as an input and the corresponding GPIO signal is low (or high if the corresponding GP_INV bit is set). If the corresponding GPI[n]_EN bit is set in the GPE1_EN register, and the GPI[n]_STS bit is set, then: • If the system is in an S1_S5 state, the event will also wake the system. • If the system is in an S0 state (or upon waking back to an S0 state), an SMI# or SCI will be caused, depending on the GPI_ROUT bits for the corresponding GPI. 0 = Each bit is cleared by writing a 1 to the bit position when the corresponding GPIO signal is not active. (The status bit will not be cleared if writing a 1 to the bit position while the signal is still active).

GPE1_EN—General Purpose Event 1 Enable Register

Bit	Description
15:0	**GPI[n]_EN.** These bits enable the corresponding GPI[n]_STS bits being set to cause an SMI#, SCI, and/or wake event.

Wake On USB

CUC2000

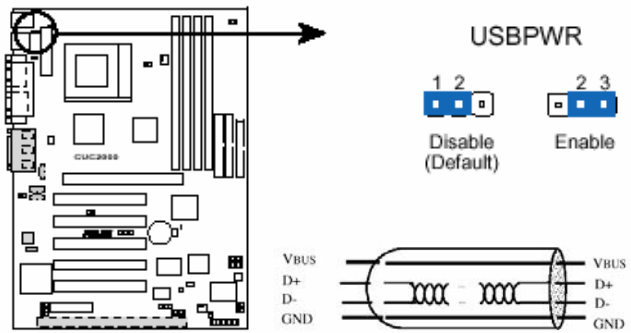
Wake On USB

- +5VSB (ATX Srandby Power) is supplied to USB ports by jumper setting

2) USB Device Wake Up (USBPWR)

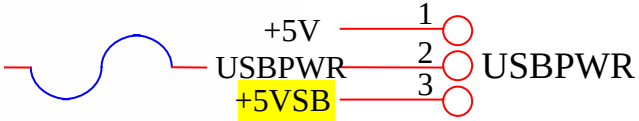
This allows you to disable or enable the USB device power up function. Set this jumper to *Enable* if you wish to use your USB device to wake up your computer. This feature requires an ATX power supply that can supply at least 2A on the +5VSB lead. The default is set to *Disable* because not all computers have the appropriate ATX power supply. Your computer will not power ON if you set this to *Enable* and do not have the appropriate ATX power supply. **NOTE:** This jumper must be set in conjunction with *Wake On USB Device* in ***4.5.1 Power Up Control.***

Setting	USBPWR
Disable	[1-2] (default)
Enable	[2-3]

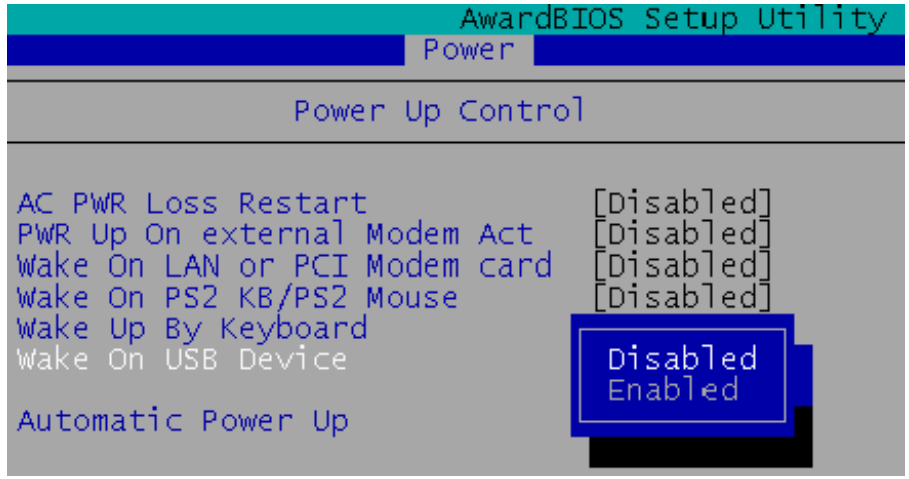


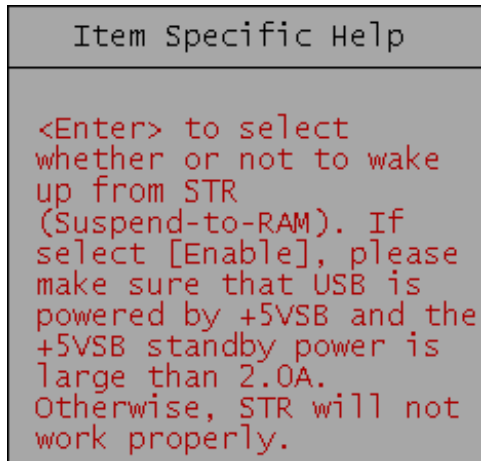
CUC2000 USB Device Wake Up

1 USB : at least 500mA
4 USB : at least 2A

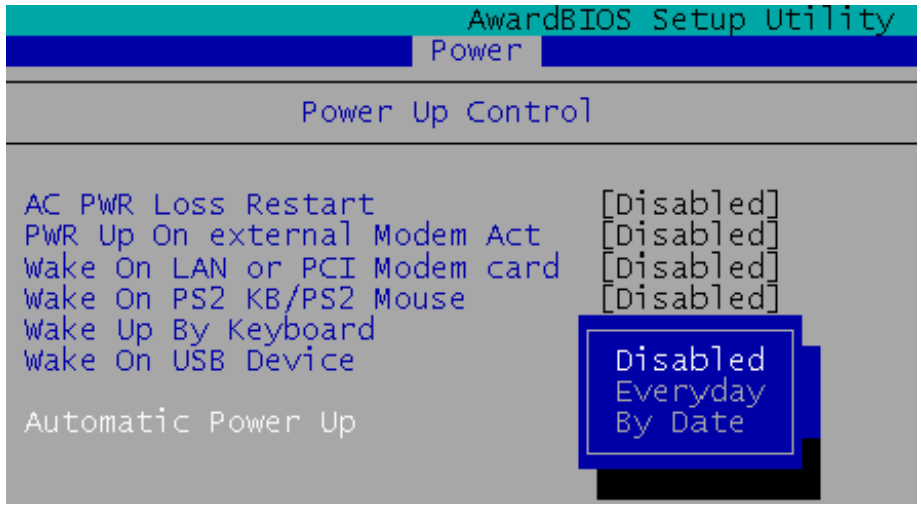


Fuse 2
(Poly Switch)





Automatic Power Up



PM1_STS—Power Management 1 Status Register

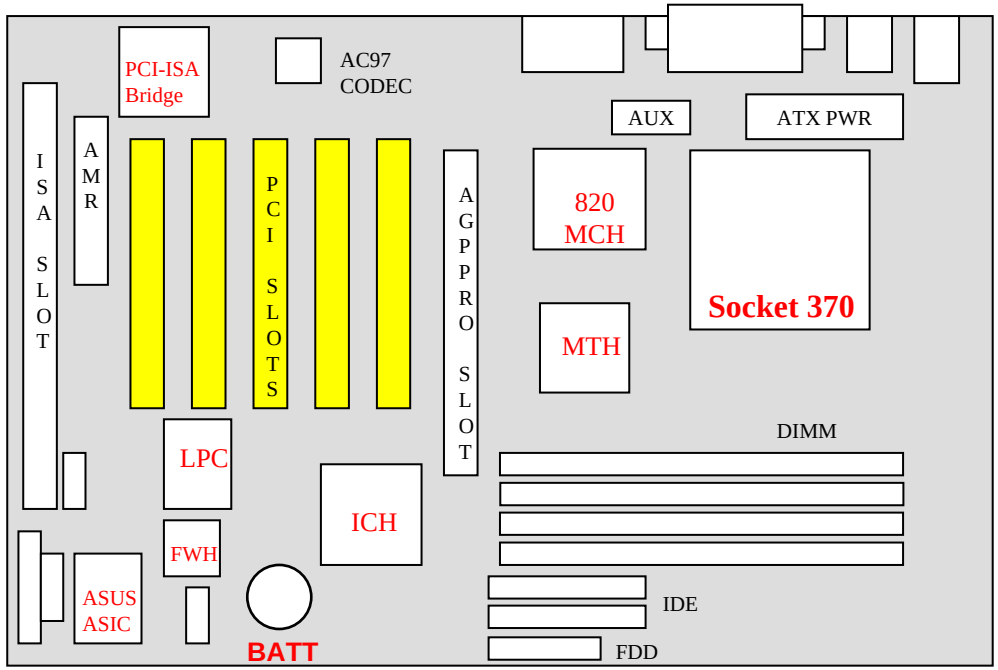
If bit 10 or 8 in this register is set, and the corresponding _EN bit is set in the PM1_EN register, then the ICH will generate a Wake Event. Once back in an S0 state (or if already in an S0 state when the event occurs), the ICH will also generate an SCI if the SCI_EN bit is set, or an SMI# if the SCI_EN bit is not set.

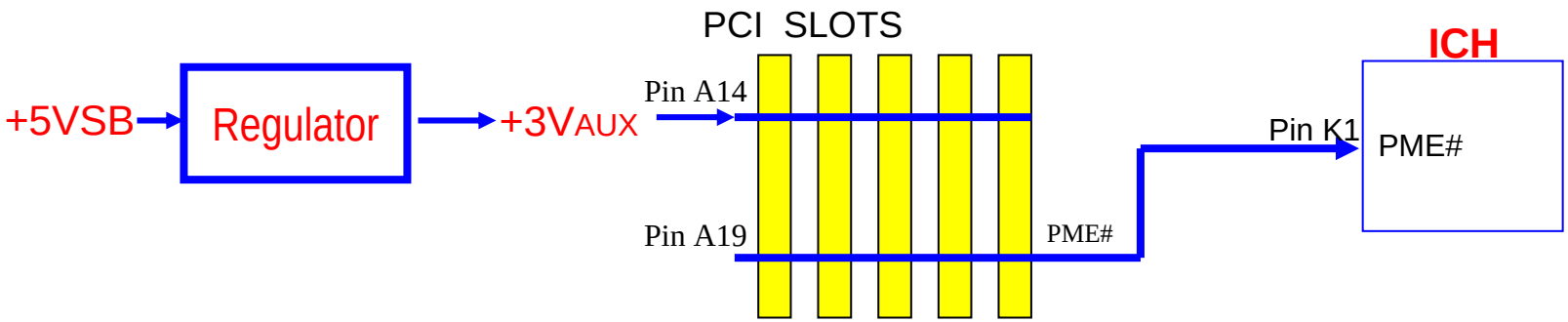
Note: Bit 5 does not cause an SMI# or a wake event. Bit 0 does not cause a wake event but can cause an SMI# or SCI.

Bit	Description
10	**RTC_STS.** 1 = This bit is set by hardware when the RTC generates an alarm (assertion of the IRQ8# signal). Additionally, if the RTC_EN bit is set, the setting of the RTC_STS bit will generate a wake event. 0 = Cleared by writing a 1 to this bit position. **NOTE:** This bit is not affected by hard resets caused by a CF9 write, but is reset by RSMRST#.

PME# and 3.3V VAUX of PCI 2.2

- PCI 2.2 adds two more pin definitions:
  - PME# (pinA19)
  - 3.3V VAUX (pin A14)
- PME = Power Management Event
  - active low, open-drain, shared
- VAUX = Auxiliary Power





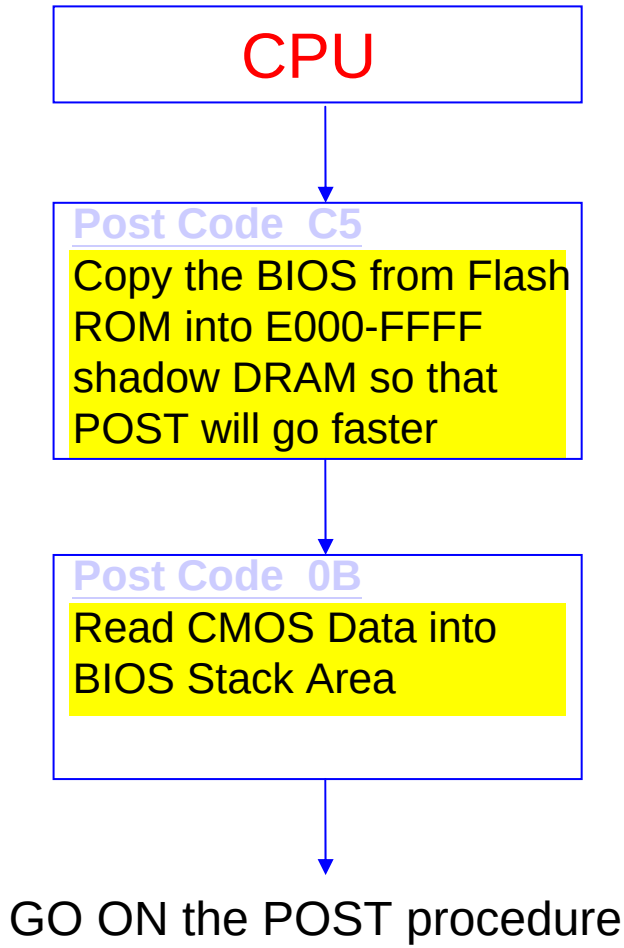
4. POST

Power On Self Test

- POST
  - Power On Self Test

- When Power is ON, the CPU will be RESETed. And the first step of CPU is to read the BIOS and to run the code.
  - And then , each step will show a POST code to port 80, while the CPU is executing the codes.
    - ➔POST CODE

- We can view the POST code to identify where the CPU stops, if happened.



POST Controller

- POST
  - Power On Self Test

- After the BIOS code has been completely executed, the BIOS will load the first sector of mass-storage device.
  - CPU loads the Operating System (OS).

CPU

↓

Post Code C5
Copy the BIOS from Flash ROM into E000-FFFF shadow DRAM so that POST will go faster

↓

Post Code 0B
Read CMOS Data into BIOS Stack Area

↓

GO ON the POST procedure

↓

Post Code 50
Write all the CMOS values currently in the BIOS stack areas back into the CMOS

↓

Post Code 63
Clear Memory that has been used .

↓

POST Code FF (Finished)

↓

LOAD OS (DOS, Win9/X,2000)

Award PnP BIOS Postcode

Post (HEX)	Descriptions
C0	1.Turn off OEM specific cache, shadow..... 2.Initialize all the standard devices with default values Standard devices includes: • DMA controller (8237) • Programmable Interrupt Controller (8259) • Programmable Interval Timer (8254) • RTC chip
C1	Auto detection of onboard DRAM & Cache
C3	1.Test the first 256K DRAM 2.Expand the compressed codes into temporary DRAM area including the compressed system BIOS & Option ROMs
C5	Copy the BIOS from ROM into E000-FFFF shadow RAM so that POST will go faster
01-02	Reserved
03	Initialize EISA registers (EISA BIOS only)
04	Reserved

Flash the BIOS

Q3. My BIOS chip is dead! What do I do?

A :

- IF BIOS EEPROM can still be flashed :

1. Please find a working PC.
2. Download BIOS flash utility (aflash21.exe is recommended) and BIOS image file for your motherboard from ASUS web site, save them into a bootable floppy disk without autoexec.bat & config.sys files.
3. Boot the system into DOS mode with the floppy disk.
4. CAREFULLY take out the BIOS EEPROM from the motherboard.
5. Plug the faulty BIOS EEPROM into the socket.
6. Proceed with bios flashing procedure.
7. After the BIOS is successfully flashed into the EEPROM, take it out and put the original EEPROM back.

✉ After the POST, the BIOS will locate at F000:0000 area.

◆ When the OS has been loaded, the BIOS will not be read/written again, unless flashing.

Flash the BIOS

STEP 1

- Place the bracket on the BIOS chip socket. Then insert the bootable BIOS chip.
- Boot the system into real DOS mode.

STEP 2

- Remove the bootable BIOS chip of the working motherboard.

STEP 3

- Place with the unbootable BIOS chip.
- Run Aflash.exe (flashing utility) under real DOS mode.